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ADVANCED DESIGN OF HIGH PERFORMANCE AND LOW COMPLEXITY 16X16 QCA MULTIPLIER

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Abstract

Low power issues have become an significant factor than area and speed in modern VLSI design. However, diverse implementation technologies near different power optimization opportunities. Low power digital Multiplier devise based on bypassing technique primarily used to reduce the switching power dissipation. while this technique offers great dynamic power savings primarily in array multipliers, due to their regular interconnection idea, it misses the reduced area and high speed recompense of tree multipliers. Therefore, mixed fashion architecture via a traditional tree based part shared with a bypassarray based part is proposed. Multipliers oblige an imperative responsibility in today's digital signal processing and various other applications. This paper proposes a QCA based 16x16 array multiplier architecture to optimize the prototype gate count. As transistors dwindle in size more and more of them can be accommodated in a single die thus escalating chip computational capabilities. However, transistors cannot get much less significant than their current extent. Quantum dot Cellular Automata (QCA) approach represents one of the feasible solutions to conquer the physical limits.

Keywords: Quantum-Dot Cellular Automata (QCA), Majority gate, Franklin logic, Half adder, Full adder.

1. Introduction

Quantum-Dot Cellular Automata (QCA) technology provides a shows potential opportunity to trounce the imminent limits of conventional CMOS technology. For this reason, in recent years the devise of logic circuits based on QCA has customary a great deal of attention, and special efforts have been directed towards arithmetic circuits, such as adders, multipliers, and multipliers. Even though multipliers are key elements for a wide range of applications QCA implementations existing in the literature are mainly provided for comparing two single bits. Only few types of

multipliers able to process n-bit operands, with n > 2 are available. The multiplier described simply computes the XNOR function to establish whether two input bits a and b match each other. The structures proposed provide higher computational capabilities and the circuits are able to separately recognize all the three possible conditions (a = b, a > b, and a<b).The 1-bit implementation proposed was then improved has been exploited in to design a parallel n-bit full multiplier. An example of serial structures is provided, whereas the n-bit multiplier described can recognize only the case in which A and B being the n bit inputs. Alternative QCA implementations of 1-bit full multipliers were recently proposed. With respect to other QCA designs, the final demonstrate reduced delays, area tenure and number of worn cells. The first is the inherent latching in wires. In essence, the wires are shift registers. This adds a new dimension to designing QCA circuits rather than CMOS circuits, allowing a designer to pipeline at every new level. Connected to this inherent latching and pipelining, the second feature of QCA is the close connection between layout and timing. There is an upper and lower bound on the size of clocking zones. Distance and time are very tightly coupled. Finally, bits in QCA designs are forever in activity. The clock and the cells are ended of unusual technologies. Perchance in the hope it may be viable to have the circuit influencing the maneuver of the clock but for the designs offered in this thesis, it is implicit that once the clock starts administration it continues to manage independently. The fundamental entity of QCA is the QCA cell, which is tranquil of four quantum dots. The cell is exciting with two superfluous electrons, which lean to inhabit diagonally contrasting dots as a result of their columbic repulsion. The electrons are tolerable to jump amid the assorted quantum dots in a cell by the system of quantum mechanical tunneling but they are not allowed to tunnel among two individual cells. Thus, there are two feasible arrangements denoted as cell polarization P=+1 and P=–1. By via cell polarization, P=+1 is to symbolize logic 1 and P=–1is to represent logic 0 and so the binary information can be preset. Arrays of QCA cells canister be arranged to achieve wire and the entire logic functions. Instead of the traditional metal wire, the QCA wire is worn to construct a digital logic circuit. In a QCA wire, the binary indicator propagates from input to output since of the electrostatic interactions between the cells. There are two kinds of QCA wires. One is a binary lead implemented amid the cells of 90 º orientations and the ancillary is an inversion fetter implemented with the cells of 45º orientation. Each unit in the inversion shackle takes on the opposite polarization of its neighbors. The QCA implementation of the anticipated full multiplier is simulated by the QCA Designer apparatus. The following parameters are used for a bistable estimate: cell size=18 nm×18 nm, number of samples=12,800, radius of effect=65 nm, relative

permittivity=12.9, convergence tolerance=0.0001, clock high=9.8e–22J, clock low=3.8e–23J, clock amplitude factor=2, layer separation=11.5 nm and maximum iterations per sample=100. Also, the diameter of the quantum dot is 5 nm and the cell reserve is 2 nm. A QCA is a nanostructure having as its vital cell a square four quantum dots structure exciting with two free electrons proficient to tunnel during the dots in the cell. Because of Columbic repulsion, the two electrons will forever dwell in contrary corners. The locations of the electrons in the chamber (also named polarizations P) establish two probable stable states that can be coupled to the binary states1 and 0.while adjacent cells intermingle through electrostatic forces and lean to align their polarizations, QCA cells do not have intrinsic dataflow directionality. To accomplish handy data directions, the cells within a QCA design are partitioned into the so-called clock zones that are gradually allied to four clock signals, each phase shifted by 90°. This clock scheme, named the zone clocking plot, makes the QCA designs inherently pipelined, as each clock precinct behaves like a D-latch as shown in figure 1.

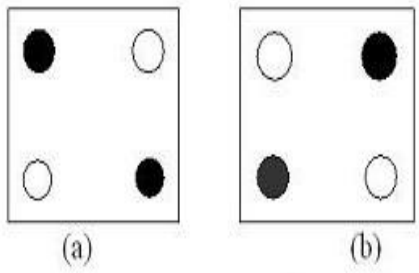

Fig. 1. QCA with Four Quantum Dots (a) Cell with Polarization p=-1 (Logic '0') (b) Cell with Polarization p=1 (Logic '1').

In section II a brief details of proposed work compare with existing work is given. In section III Results and Discussion are shown. Concluding remarks are presented in Section IV.

2. Related Work

A. Majority Gate

QCA cells are worn for both logic structures and interconnections that can utilize either the coplanar fractious or the bridge performance. The primary logic gates innately accessible within the QCA technology are the inverter and the MG. The QCA cells are 18-nm extensive and 18-nm elevated; the cells are sited on a grid with a cell center-to-center reserve of 20 nm; there is at slightest one cell spacing amid adjacent wires; the quantum-dot diameter is 5 nm; the multilayer wire voyage structure is oppressed as shown in figure 2.

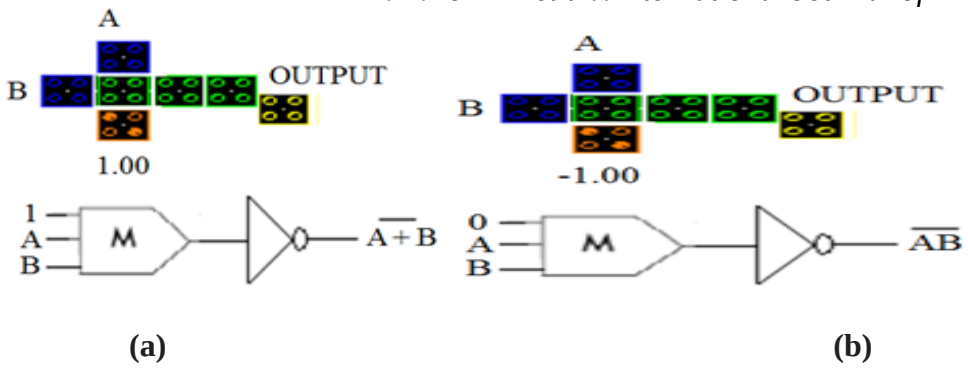

Fig. 2. (a) Layout of NOR gate (b) Layout of NAND gate.

To implement more convoluted logical functions, a division of simple logical gates is mandatory. For example, it would be impossible to implement an XOR gate, code converters, pseudo-code generators, parity generators, and checkers in QCA without a logical AND gate, OR gate, or else inverter. It has been demonstrated that a value's complement can be obtained simply by ripping it to a 450 wire at the proper location. Implementing the logical AND and OR functions is also quite simple by fixing the polarization to one of the inputs of preponderance vote as logic '1' or '0', we can obtain an OR gate and an AND gate respectively. NOR gate and NAND gates can be implemented by complementing OR gate plus an AND gate respectively. NOR entry is realized by allied OR gate followed by inverter shown in figure 2(a). Similarly, NAND gate is realized by connected AND gate followed by inverter shown in figure 2(b).

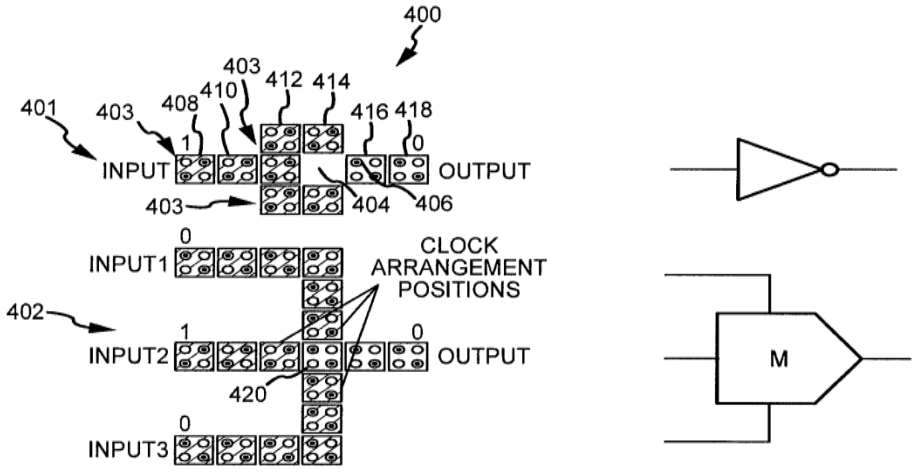

Fig. 3. Majority Logic Architecture.

The input bits are applied to the majority logic architecture. This architecture is used to find the more number of ones and zeros in the input bits. This architecture is used to find the majority for 3-bit input functions and to modify the architecture using the Boolean equations. This architecture is mainly used to the fast comparison process for given more number of bits. The majority architecture is the basic component for the multiplier architecture as shown in figure 3.

B. Franklin Logic

The FRANKLIN logic function is one of the optimization technique for the majority logic architecture. The optimization technique is mainly based upon the Boolean logic function. The modified Boolean logic function processed by the FRANKLIN logic optimized function is applied to the majority logic gate architecture.This technique is used to reduce the gate pattern count for majority architecture.In this project, number of gates used in the majority gate architecture have been reduced to four from five gates using this Franklin logic function as shown in figure 4.

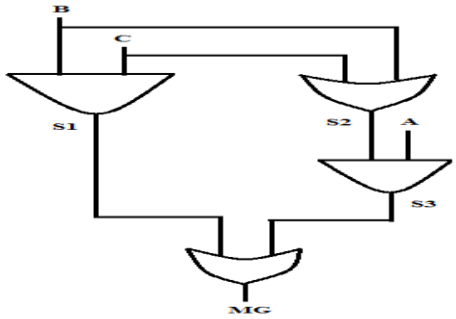

Fig. 4. Majority Gate based on FRANKLIN Logic Function.

C. 16X16 QCA Array Multiplier

The 32 bit multiplier architecture can be structured using the QCA modules which are implemented using the reduced majority gate architecture by FRANKLIN logic function block diagram as shown in figure 5.

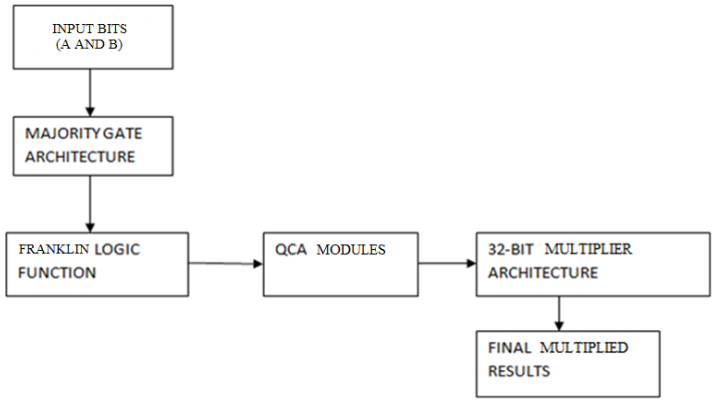

Fig. 5. Block diagram of Franklin logic function.

QCA module is used to enhance the multiplication process by developing the speed when compared to the existing system.QCA module is based on the fact that basic building blocks using majority gates are capable of representing only one bit of data and the spatial arrangement is used to implement the logic function AND and OR as shown in figure 6 and 7.

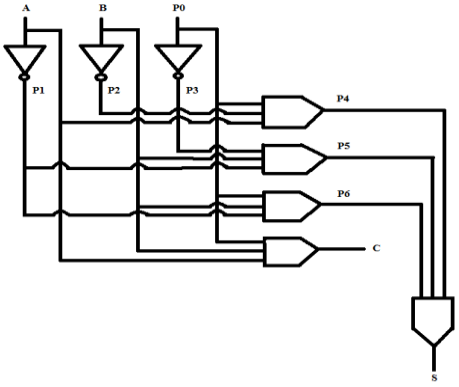

Fig. 6. Half Adder using MG.

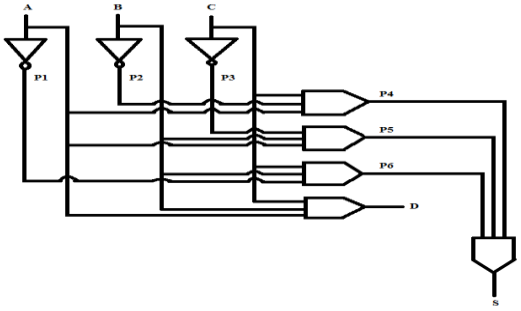

Fig. 7. Full Adder using MG.

The 32 bit multiplier architecture is designed using four-dot QCA cell modeling approach by using a specific electron configurations to represent the logic values 0 and 1.The design process resulted in the implementation of binary wire and the ability to transfer data in the functionality complete set of logic functions enables the construction of any switching structure as shown in figure 8.

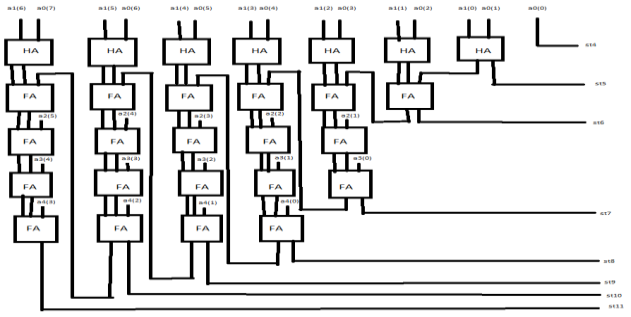

Fig. 8. 8x8 Array Multiplier Using QCA.

A 8x8 array multiplier consists of 64 AND gates, 8 HAs, 48FAs (total 56 Adders) is shown in Fig 4.13.Therefore, for an m x n Array Multiplier, m*n AND gate, n HAs, (m-2)*n FAs, i.e. a entire of (m-1)*n adders are mandatory. Fig 4.13 also illustrates generation of partial products in a 8x8 array multiplier. Similarly, a 16 x16 array multiplier takes 16- bit

multiplicand and 16- bit multiplier and generates32 partial products. The two 16 bit inputs are given to the majority gate architecture. This majority gate architecture initially composed of five gates. Using FRANKLIN logic function, this majority gate architecture composition can be reduced to four gates. In the QCA module, half adder and full adder can be structured using the reduced majority gate architecture and this prototype can be extended to 32 bit multiplier architecture.

3. Results and Discussion

A and B are the two 16 bit inputs given to the muliplier architecture and C is the 32 bit output obtained using QCA modules which is composed of majority gates and inverteras shown in figure 9.

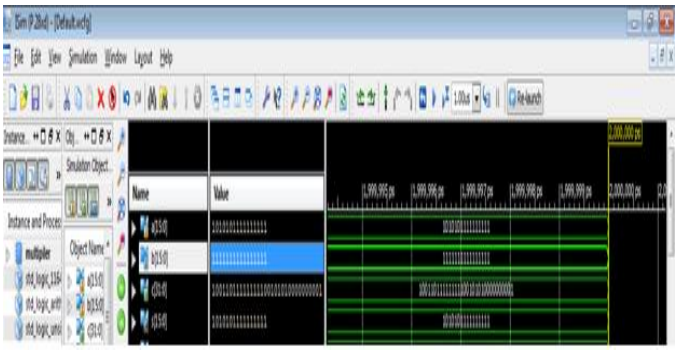

Fig. 9. Simulation output of 16x16 multiplier using QCA.

This shows Register Transfer Level Schematic of 16*16 Multiplier which multiplies two inputs. This RTL Schematic consists of only AND and OR gates as shown in figure 10.

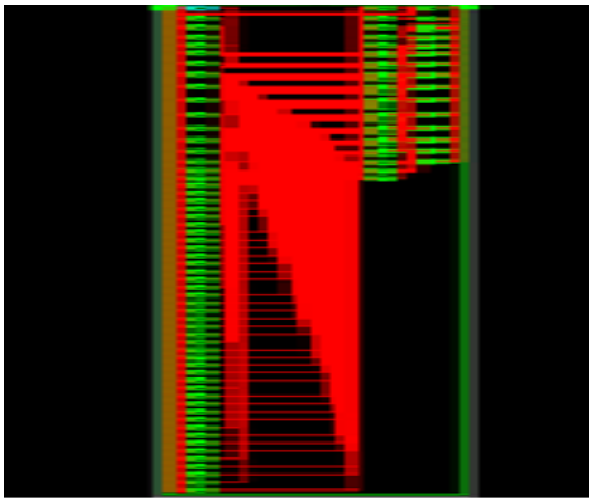

Fig. 10. RTL Schematic of 16x16 Multiplier.

This is the Technology Schematic of 16**x**16 Multiplier which multiplies two inputs. This Technology Schematic consists of Look up table (LUT) which shows the gate architecture as shown in figure 11.

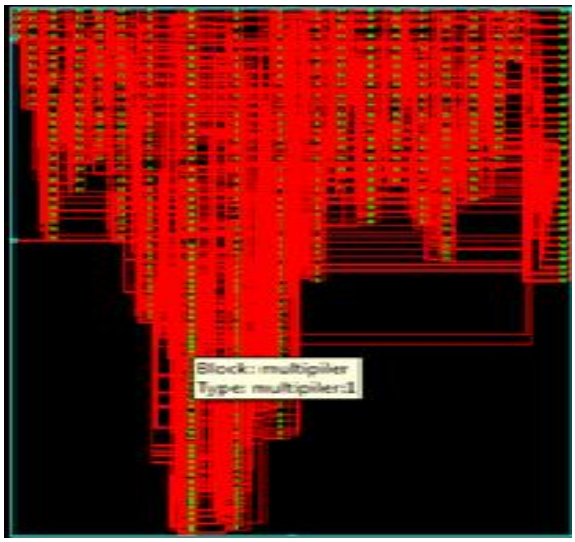

Fig. 11. Technology Schematic of 16x16 Multiplier.

This is the Wallace Multiplier paper which shows dynamic power in micro watts and delay in nano seconds. Dynamic power obtained is 6.34mW and Delay obtained is 46ns. In the existing system, Wallace multiplier with the combination of CSA consumes 6.34mW of power and delay of 46ns. In the existing system, Booth multiplier consumes 636 LUTs and 100 IOs. In the proposed system, 32 bit MG Multiplier using QCA consumes 5.2mW of power, 25.173ns of delay, 547 LUTs and 64 IOs as shown in table 1.

Table. 1. Comparison table to show the power reduction.

Features	**Wallace Tree Multiplier**	**Booth Multiplier**	**MG Multiplier Based On QCA**
POWER	6.34mW	151.34	5.2mW
DELAY	46ns	46.7	25.173ns
NO. OF LUTs	769	636	547
NO. OF IOs	20	100	64

This paper presented the construction of 32 bit Multiplier based on QCA for high speed and low power dissipations. QCA is the emerging nano-technology which is mainly used instead of CMOS technology. Majority gate and inverter are the main inherent gates present in the QCA. It is very effective when simulation is done in the main QCA kit. Since it is very expensive, it is very difficult to implement in the QCA kit. Hence we have used the QCA prototype in the Xilinx coding to run the simulation.

4. Conclusion

An optimized QCA full multiplier was proposed. The proposed multiplier is simulated using the QCA Designer tool, and the simulation results show that the logical function of the designed circuit is correct. The optimized QCA full multiplier shows improvement in terms of power consumption, cell count, and delay. In comparison with the best previous Wallace multiplier, our design has 64% and 85% improvement in the cell count and the area, respectively. Also, our multiplier is faster than previous ones. A new methodology has been presented to design binary multipliers in QCA. It is based on innovative formulations that allow augmented speed performances and compact overall sizes to be achieved with revere to the existing competitors.

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