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DESIGN OF FIR FILTER ARCHITECTURE USING VARIOUS EFFICIENT MULTIPLIERS

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Abstract

In any communication system filters perform a major role. The output response of any communication system is depends on the FIR filter, so need a perfect filter, to get an efficient response. Multiplier is one of the important blocks in FIR filter, so need an efficient and perfect response multiplier design. Multiplier is one of the basic building blocks in the digital circuits. So the performance of the multiplier is important to get an efficient circuit design. Power consumption is one of the major drawbacks in the multiplier. Power consumed by the multiplier is higher in the digital circuits. The Wallace tree multiplier used in the filter provides some drawbacks. The drawbacks in the Wallace tree multiplier are delay, power consumption and area consumption. To overcome the drawbacks in the Wallace tree multiplier, to design a new multiplier named as Birecoder multiplier. This multiplier reduces the stages of partial product addition. So this multiplier takes less number of gates to implement and also it overcomes the drawbacks of Wallace tree multiplier. Multiplier design is done by verilogHDL. Finally the designed birecoder multipliers are applied into the FIR filter, and show the best filter.

Keywords: Low power multiplier, Reversible Logic gates, Digital circuits, Verilog HDL

Introduction

Finite-impulse response (FIR) filters play an important role in many communication systems. The variety of tasks such as noise cancellation, matched filtering, interference cancellation, attenuation reduction, channel equalization, etc. Different types of architectures and implementation methods were proposed to improve the performance of filters. One of the most used operations in digital signal processing is Finite Impulse Response (FIR) filtering. FIR filter structures are reduced the number of operation like additions, subtractions, shifting; multiplication. Reconfigurable FIR filter structural designs were done for low power applications. Multiplications are important

operations in FIR filters. But the weight of the filter is constants. Several techniques were developed over the years for the efficient realization of constant multiplications by a network of add and subtract, shift operations. Constant multiplication methods are classified into two types first is single constant multiplication (SCM) methods and second one is multiple constant multiplication (MCM) methods. Single constant multiplication methods are applied to multiply a variable operand with a known constant, where the multiplications are realized by a number of add, sub and shift operations accompanied by shifting operation. Multiple constant multiplication methods are applied for multiplication of one variable operand with number of constants, the intermediate results can be shared across the entire network to minimize the overall computational complexity. In general, MCM method cannot be used directly for sample-by-sample processing of direct form FIR filters. It cannot be implemented in transposed direct-form efficiently due to its large latency for accumulation of partial results. The MCM technique is used for efficient implementation of direct form block FIR filters for high-speed or low-power applications.

Related Works

J. Chen, and W. Ding [1] have been proposed the concept of low Power digital Filter using low power multipliers and adders. This proposed method includes low power multiplier, serial adder, booth multiplier, and shift and add multipliers, folding transformation in linear phase architecture and applied to fir filters to power consumption. A. Dandapat et al. [2] was presented a concept of High-performance FIR Filter architecture for fixed and reconfigurable applications. Transpose form finite-impulse response (FIR) filters are pipelined and support multiple constant multiplications (MCM) technique.

Gowrishankar et al [3] have been proposed Reconfigurable filter architecture for static and Dynamic Power Consumption. When the filter order is fixed and not changed for particular applications, and filter performance can be made using the proposed architecture. The power savings is up to 40.3% with minor degradation, and the area overhead of the proposed scheme is less than 4.9%. T. Hentschel et al. [4] presented a novel concept of Design of area and power efficient digital FIR Filter using modified MAC unit. The design of digital finite impulse response (FIR) filter for digital signal processing (DSP) in this project shows Power Delay Product (PDP) is improved by 16.80% and 12.54%.

Wallace Tree Multiplier Design

Array multiplication is performed by using Wallace tree multiplier Wallace multiplication is also knows as parallel multiplier. Parallel array multiplier performs operation using more number of gates and it occupies large area. To

reduce this problem, Wallace tree multiplier is designed; the multiplier design was done by using proposed SQRT CSLA. To improve the speed by modify the Carry select adder using D-FF by replacing the BEC. Ripple carry adder and BEC are used in the carry select adder. The Conventional Group2, Group3 and Group4 structures used normal full adder, half adder, BEC Converter and MUX. Conventional SQRT CSLA provides lower latency and high speed than the previous architectures.

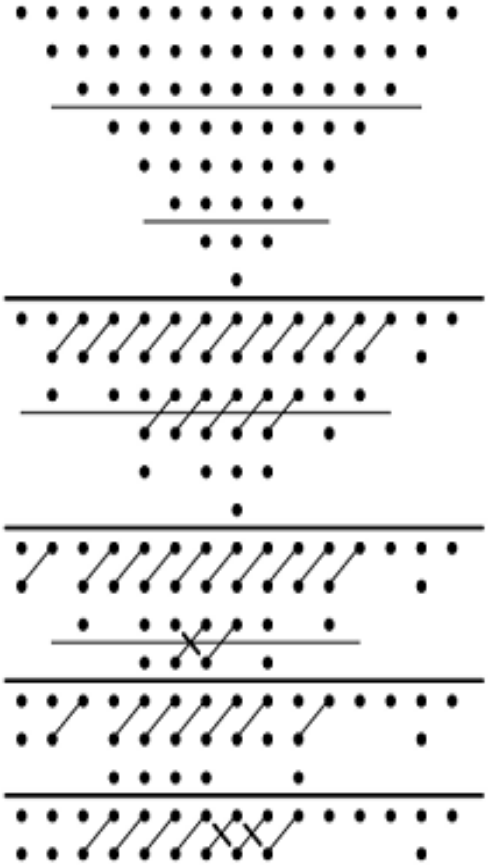

Figure. 1 Structure of reduced complexity Wallace tree multiplier.

Figure.1 shows Wallace multiplier structure. The Wallace tree multiplier has reduced number of half adders, full adders when compared to the conventional multiplier. In the modified multiplier circuit, AND gates in the partial products are arranged in an inverted triangle order. The operation is divided into three row groups in the reduced complexity Wallace multiplier. Full adder is used for adding three bits.

Design of Proposed Birecoder Multiplier

In general partial product generation stages are decide the speed of the operation. To reduce the steps in the partial product generation the performance of the multiplier is automatically increased. In eight bit Bi-Recoder multiplier, the partial products stages were done by using multiplexer. Mux is used to perform the PPG process based on multiplier bit values. Multiplicand value is directly passed to first input of 2:1 Mux and 8-bit of zero's are given to

another input of 2:1 Mux. Multiplier value is given to the selection line of Mux. In every stage, single bit of multiplier is considered as selection input of Multiplexer. If it is zero, Mux passes '0' to output else if it is one, Mux passes the multiplicand value to output. Based on the selection line given to input of multiplexer, the output is generated.

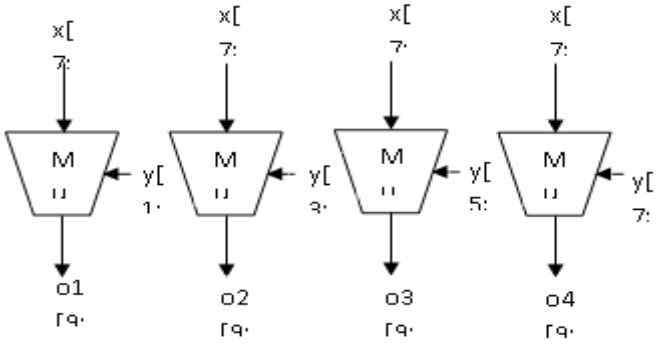

Figure. 2 Partial Product Generation process of Bi-Recoder Multiplier.

In fig.2 shows the partial product generation stages of Birecoder multiplier. 'x' represents multiplicand value and the value of 'y' represent the multiplier value. For each multiplexer produces 10-bit partial product value. Multiplier bits are divided into 4 groups and each group is having two bits for selection line input.

Proposed Fir Filter Structure

Finite Impulse Response (FIR) filter is used to filter the unwanted noise signal, attenuation and unwanted signals at finite impulse durations. Multiplication and Accumulation (MAC) unit determine the time of periodic impulses. High performance MAC unit is required to improve the performance of the digital FIR filter. Square root CSLA based Bi-Recoder multiplier is implemented into the direct form FIR filter. So we can improve the performance of digital FIR filter. The performance is analyzed by using the simulation environments.

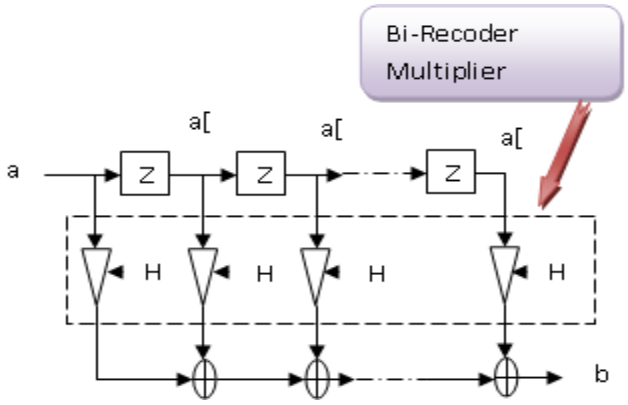

Figure. 3 Structure of Direct Form FIR Filter.

In fig.3 shows the structure of the direct form FIR filter, the figure clearly explain the operation of FIR filter. Output of the filter based on the number of order used in the filter structure. Each order of the filter using one multiplier.

Based on the multiplier operation the performance of the filter is achieved. Here using the Birecoder multiplier for multiplication operation. This multiplier produced the better results during the filtering operation.

Simulation Results

Simulation was done by using the ModelSim XE III 6.3c simulator. Parameters like area delay and power can be analyzed by using Xilinx ISE 10.1 simulator. Output of the Vedic multiplier is same as other multiplier, compared to the other multiplier speed and accuracy of the Vedic multiplier is higher. The result is shown in the figure. 4 contains different combination of inputs, based on the input it produced the output.

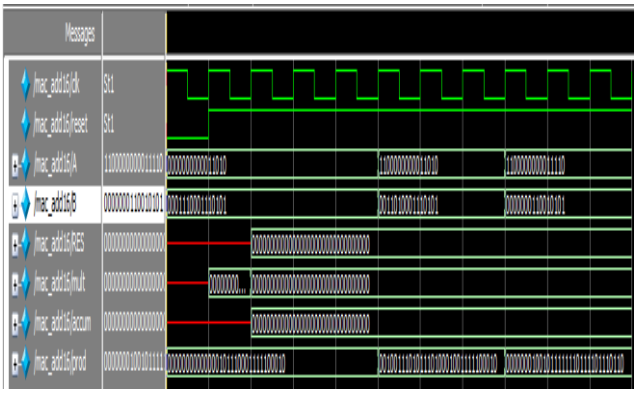

Figure. 4 Simulation Output.

Performance Evaluation and Comparison.

Table No.1: Comparison of Area and Delay between Existing and Proposed system.

Parameters	Existing Wallace Tree Multiplier	Proposed Bi-recoder Multiplier
LUTs	145	131
Slices	95	73
Delay(ns)	21.445ns	20.170ns
Power(mW)	896mW	748mW

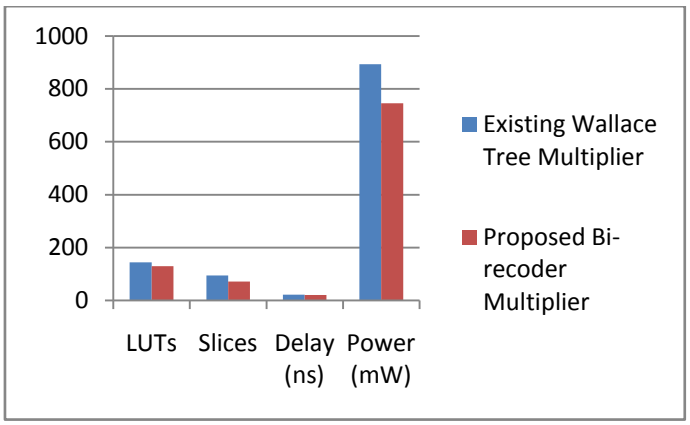

Figure. 7 Graphical representations of Area, Delay and power.

In fig.7 shows the difference in existing and proposed multiplier design. It is clearly explain the parameters are reduced when compared to the previous multiplier design.

Conclusion

An area efficient and high speed multiplier Birecoder multiplier was designed. It reduces the area complexity, latency and high power dissipation in the digital circuits. The proposed multiplier was applied to the direct form FIR filter for verifying the filter operation. After applying the multiplier into the filter, the performance is evaluated. It provides the better results when compared to the other FIR filters. Now the filter is applicable for much application like digital signal processing, wireless communication, image processing etc. The modified FIR filter is suitable for all kind of applications.

Reference

1. J. Chen, C. H. Chang, F. Fen., W. Ding, and J. Ding, (2014) "Novel Design Algorithm for Low Complexity Programmable FIR Based on Extended Double Base Number System", IEEE Transaction on Circuits and Systems, Vol. 62, Issue. 1, pp: 1-10.
2. A. Dandapat, S. Ghosal, P. Sarkar and D. Mukhopadhyay,(2010) "A 1.2- ns16×16-Bit Binary Multiplier Using High Speed Compressors", World Academy of Science, Engineering and Technology.
3. V. Gowrishankar, D. Manoranjitham, and P. Jagadeesh,(2013) "Efficient FIR Filter Design Using Modified Carry Select Adder & Wallace Tree Multiplier" International Journal of Science, Engineering and Technology Research (IJSETR), Vol. 2, Issue. 3, pp: 703-711.
4. T. Hentschel and G. Fettweis,(1999) "Software radio receivers," in CDMA Techniques for Third Generation Mobile Systems. Dordrecht, The Netherlands: Kluwer, pp. 257–283.
5. Jagadeshwar Rao M and Sanjay Dubey, (2012) "A High Speed Wallace Tree Multiplier Using Modified Booth Algorithm for Fast Arithmetic Circuits", IOSR Journal of Electronics and Communication Engineering, vol. 3, no. 1.
6. C. U. Kumar, and B. J. Rabi,(2014) "Area efficient FIR filter using graph based algorithm", In Current Trends in Engineering and Technology (ICCTET), 2nd International Conference, pp: pp. 495-498, IEEE.
7. X. Lai, and Z. Lin,(2014) "Optimal Design of Constrained FIR Filters Without Phase Response Specifications", IEEE Transactions on signal processing, Vol.62, Issue. 7, pp: 4532-4546.

8. E. Mirchandani, R. L. Zinser, Jr., and J. B. Evans,“ A new adaptive noise cancellation scheme in the presence of crosstalk [speech signals],” IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process., vol. 39, no. 10, pp. 681–694.
9. M.Moris Mano,(2002) “Digital Design”, Pearson Education, 3rd edition.
10. J. G. Proakis and D. G. Manolakis,(1996) Digital Signal Processing : Principles, Algorithmsand Applications.UpperSaddle River, NJ,USA: PrenticeHall.