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DESIGN AND IMPLEMENTATION OF MULTIPLIER CIRCUITS USING REVERSIBLE LOGIC GATES AND ESTIMATION OF POWER DISSIPATION

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Abstract

Reversible logic is one of the important technologies for low power dissipation. Reversible logic gates aims at optimizing the delay, area and power consumption. The normal set of gates such as the NAND, AND, NOR, OR, XOR and XNOR are not reversible because number of inputs and outputs are not equal, in reversible logic gates number of inputs is equal to number of outputs. Some of the reversible logic gates are Feynman gate, Fredkin gate, Double Feynman gate, Toffoli-Gate, Peres gate and HNG gate. Power consumption is one of the major drawbacks in the multiplier. Power consumed by the multiplier is higher in the digital circuits. To overcome the power consumption problem by design an efficient low power multiplier. The low power multiplier is designed by using reversible logic gates. Generally reversible logic was designed by avoiding the higher power consumption by the circuits, compared to Irreversible logic gates, reversible logic consumes less power. To apply the logic in the entire multiplier circuit and see the performance of the multiplier. The low power multipliers overcome the power dissipation in the circuits. The designed multiplier is applied into the filter and shows the filter performance. The designs are done by Verilog HDL and Implemented by Modelsim and ISE Xilinx 10.1 simulation environment. The power can be analyzed by using Xilinx X Power analysis. Finally comparison is done between the irreversible and reversible design.

Keywords: Low power multiplier, Reversible Logic gates, Digital circuits, Verilog HDL, Xilinx

Introduction

In VLSI system the Area and power-delay product become the most important metrics of performance. The reduction of the power dissipation and reduces the latency require optimization at all levels of the design procedure. Since,

most of the digital circuit is designed of simple and complex logic gates. Study the best way to implement multiplier in older to achieve low power dissipation and high speed. Reversible logic allows designers to implement the subsystem circuits design with zero power dissipation than the existing architecture design. The synthesis of reversible circuit is not easy with the increasing level of device integration and the growth in complexity of circuits, power dissipation, delay and area are the primary goals of design. The failure of high-power circuits relates to the increasing popularity of portable electronic devices. Laptop, pagers, portable video players and cellular phones all use batteries as a power source, in nature battery provide a limited time of operation before they require recharging. To extend life of battery, low power operation is implemented in the integrated circuits. Some application requires more operating power, placing greater demands on energy storage elements in the system. Limitations of Power dissipation come in two methods. The first method is related to cooling considerations of system when implementing high performance systems. High speed circuits dissipate large amount of energy in a short amount of time, generating a great deal of heat as a by-product. A gate is reversible if there is a distinct output assignment for each distinct input. Thus, a reversible gate's inputs are uniquely determined from its outputs. A reversible logic gate contains same number of inputs and outputs. Reversible gates are generating the balanced outputs. In a circuit the constant variable is used to balance the output of the circuit. A reversible logic gate contains n number of inputs and n number of outputs with n to n mapping, its helps to determining the inputs and outputs. Extra outputs are added to make the output count equal to the input counts. The main challenges of the gates are memory usage, latency, number of gates and quantum cost.

Related Works

P.vanusha et al. [1] have been proposed a concept of Low power computing logic gates design using reversible logic. Here using the reversible logic gates to designing a full adder, encoder and decoder circuit by using the tanner EDA simulation environment and calculate the power consumption with 45nm Nanometer Technology. Monika rangari et al. [2] was presented a novel concept named as design of reversible logic ALU using reversible logic gates with low delay. In this design of 1-bit reversible ALU using reversible logic gates is proposed. The proposed ALU is analyzed on FPGA SPARTAN3 device. The proposed design is compared in terms of propagation delay, number of gates and power. The four-bit reversible ALU is also design on proposed 1- bit reversible ALU architecture. Power Estimation in Binary CMOS Circuits Based on Multiple-Valued Logic have been presented by Bangyuan et al. [3] this paper proposed the use of quaternary and ternary descriptions of signal behavior for power estimation of binary CMOS

circuits. A multiple-valued-logic simulation algorithm that can be used at the circuit level, where the MOS device is replaced by a simply modeled device, as well as at the gate level. Zhijin Guan et al. [4] presented a novel concept of design constructing the Arithmetic Logic Unit (ALU) based on reversible logic gates. By using reversible logic gates replacing of using traditional logic gates, a reversible ALU function is the same as the traditional ALU. The proposed reversible ALU reduces the information losses and the power dissipation of the circuit. Bruce J W et al.. [5] proposed the concept of design and implementation of efficient adder circuits based on the fredkin gates. Fredkin and PFAG gates are proposed to design the low power full adder circuit and have lower hardware complexity. Manoj kumar K et al. was presented the efficient design and implementation of adders with reversible logic. In this paper different types of adders were implemented. The adders are carry save adder, carry skip adder, ripple carry adder, carry bypass adder. Implementation was done by both reversible and irreversible gates. The performance of the adders is analyzed in the simulation environment.

Design of Vedic Multiplier

Multiplication is one of the important arithmetic operations in many applications. One of the application are signal processing, communication etc. Signal processing involves multiplication operation, latency and accuracy is the main constraint in the multiplication operation. Speed can be achieved by reducing the computation process in the multiplication technique. Vedic multiplier is efficient multiplication technique. In-between the multiplication partial product addition is one of the important steps to perform the operations. Addition of partial products is done using two ripple carry adder. To obtain the final result by concatenating the last two bits of the first multiplier, four sum bits of the second four bit ripple carry adder and the sum bits of two bit ripple carry adder. The step by step process of the multiplication is reduces the latency of the multipliers. By reducing the latency in the design, obviously the speed of the operation is increased. So it increases the performance of the entire multiplier application.

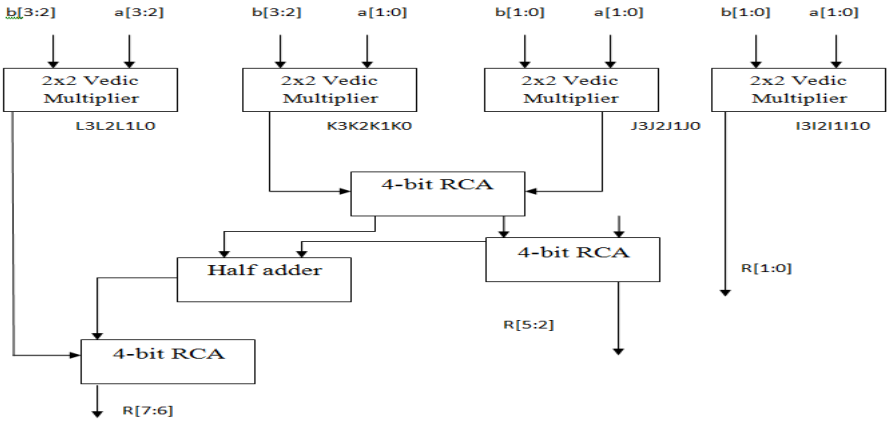

Figure. 1 Block Diagram of 4X4 Vedic Multiplier.

In fig. 1 shows block diagrammatic representation of 4 x 4 Vedic multiplier. It clearly explains the detailed operation of the Vedic multiplier. It was designed by four 2 x 2 Vedic multiplier, each multiplier perform the operation separately. Partial products are added by 8-bit SQRT-CSLA; finally get a 16-bit multiplication output. The 4-bit input sequence is divided into two 2-bit numbers. Input to the 2-bit multiplier are a[1:0] & b[1:0], a[3:2] & b[1:0], a[1:0] & b[3:2], a[3:2] & b[3:2]. Intermediate partial products output are added using the three modified adder, named as SQRT-CSLA. Carry propagation delay and low complexity are recognized as high potential in every addition circuit. To achieve an efficient output, the proposed SQRT-CSLA structure has designed. SQRT-CSLA adder circuit is classified into two types based on selecting the carry inputs. a) Dual RCA based SQRT CSLA; b) BEC based SQRT CSLA.

Reversible Logic Function

Reversible logic gate is a successful design to construct a computer with no heat generation. Reversible logic computing is also to improvement in energy efficiency of the circuit. Generally energy efficiency is to affect the speed of circuits such as nano electronic and the speed of most computing applications. To increase the portability of devices, reversible computing is required. The circuit element sizes to reduce the atomic size of the device and the devices become more portable.

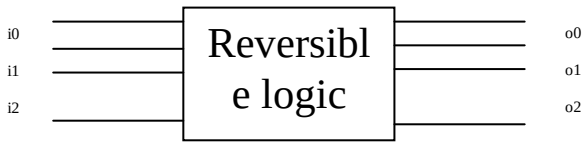

Figure. 2 Reversible Logic gate.

In fig.2 shows the structure of reversible logic gate. It contains number of inputs and number of outputs. Some of the reversible logic needs constant input and garbage output to correct the input and output. Mostly the garbage outputs are ignored in the operations. Different types of logic gates are in the reversible logic named as HNG, toffoli, peres, fredkin, TSG. These gates are mostly used for reversible logic function. Reversible logic circuit contains minimum quantum cost. The design is to produce minimum number of garbage outputs, and also have minimum number of constant inputs.

Multiplier Using Reversible Logic Gates

A four bit multiplier is designed by using reversible logic functions. To replace the functions of irreversible logic function by reversible logic function. The operation is more or less same as irreversible logic functions. It also produced the same output. The design of multiplier using reversible logic gates is done in two parts: generation of partial products and multi - operand addition.

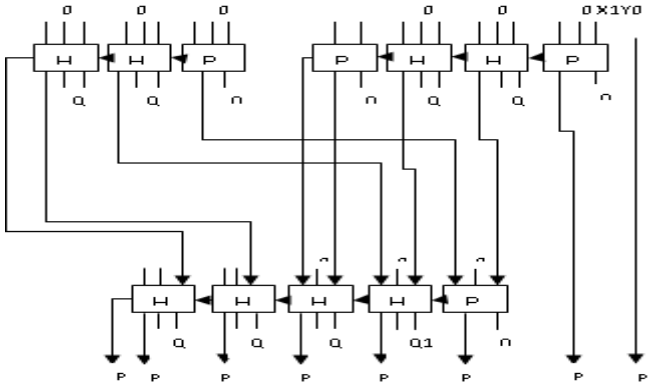

Figure. 3 Four bit multiplier using Reversible logic gates.

The circuit for partial product generation is common for both unsigned multiplier and signed multipliers. In the previous multiplier designs partial products are generated using PFAG gates, and also apply this product to multi - operand addition circuit. In the logic circuit only reduces the number of gates required to produce product terms but also provide the required number of product terms. The product terms generated from the PPG circuit are to be added to achieve the multiplier operation. In fig.3 shows the circuit diagram of multiplier design using reversible logic gates. Mostly HNG, PG are used to design the multiplier. Not only is the two gates variety of logic gates available in the design. Each logic gates have different functions and different characters. Based on the logic gates only the entire operation is performed. It is mainly used for reduce the power dissipation in the logic circuit.

Simulation Result

Simulation was done by using the Xilinx ISE 10.1. Parameters like area delay and power can be analyzed by using same simulation environment. This tool is used to analyze the RTL schematic view and layout of the design. Output of the Vedic multiplier is same as other multiplier, compared to the other multiplier speed and accuracy of the Vedic multiplier is higher. The results shown in the figure. 4 contains different combination of inputs, based on the input it produced the output.

Figure. 4 Simulation Output

Comparison between Existing and Prosed Design.

Table No. 1: Comparison between the existing and proposed design.

Parameters	Existing Vedic Multiplier	Proposed Multiplier using Reversible Logic
Power (w)	0.232 W	0.531 W
LUTs	36	37
Slices	19	21
Delay (ns)	6.21 ns	6.19ns

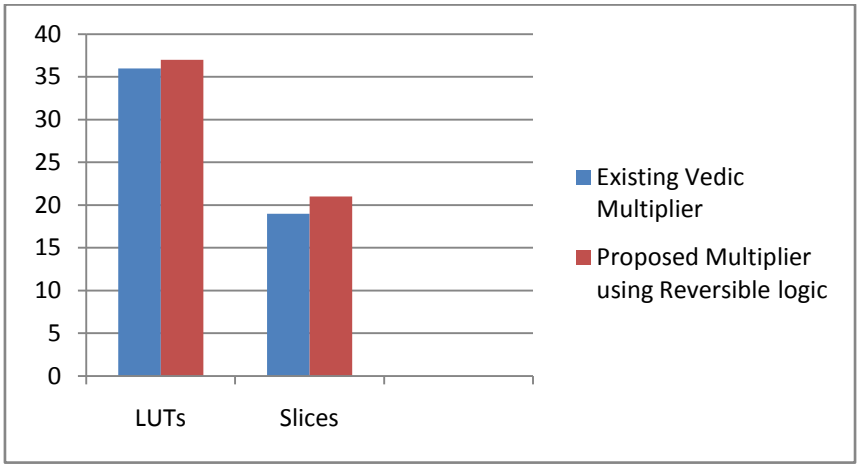

Figure. 5 Graphical Representation of LUTs and slices.

The above comparison graph clearly shows the difference of LUTs and slices. Reversible logic multiplier takes quite large LUT and slices. These one is not considered as drawback of the design.

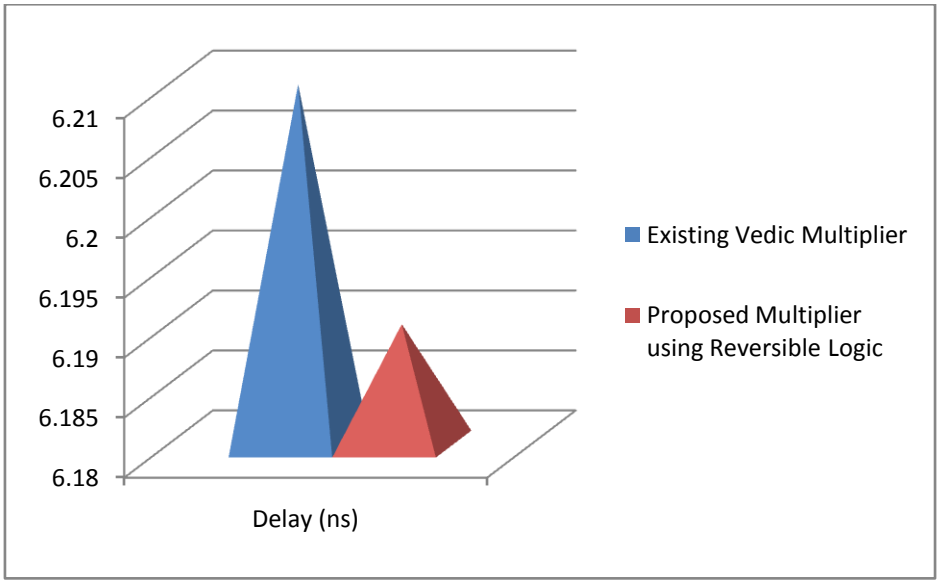

Figure. 6 Graphical Representation of Delay.

The above graph clearly shows the delay difference between the existing vedic multiplier and the proposed multiplier. Latency is reduced in the proposed multiplier. Delay measurement is taken in terms of nano seconds.

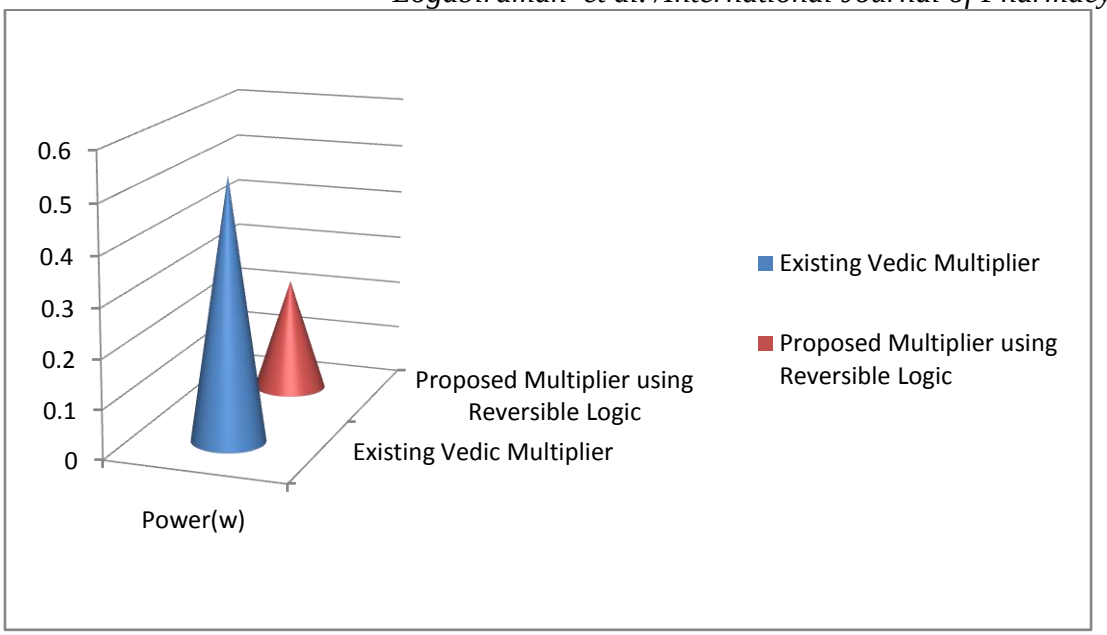

Figure.7 Graphical Representation of Power.

This graph shows the power difference between the existing multiplier and the proposed multiplier. The main purpose of the reversible logic is reduced the power dissipation. Reversible logic reduces 6% of power compared to the existing one.

Conclusion

This paper presents the implementation of four bit multiplier using reversible and irreversible logic gates. In the reversible logic gates there are no losses of information during the operation, and also the heat generation is zero. So the reversible logic gates are used to reduce the power dissipation in the circuit. The proposed multiplier design has less number of garbage outputs and small number of constant inputs. Quantum cost and the number of gates also reduced in the logic function. So the proposed logic is used for much application to reduce the power dissipation during the operation.

Reference

1. Madhusmita Mahapatro, Sisira Kanta Panda, JagannathSatpathy, Meraj Saheel "Design of Arithmetic Circuits Using Reversible Logic Gates and Power Dissipation Calculation" International Symposium on Electronic System Design(2010).
2. A.P.Hatkar,A.A Hatkar, N.P Narkhede "ASIC Design of Reversible Multiplier circuits" International Conference on Electronics system ,Signal processing and Computing technologies(ICESC),IEEE,PP.47-52,2014.
3. Monika rangari,Prof.Richa saraswat and Dr.Rita jain(April 2015) " Design of reversible logic ALU using reversible logic gates with lowdelay profile" IJARCCE papers, vol. 4,issue 4 ,April 2015.

4. Bangyuan, Chen Xunweiwu and Massoud Pedram, "Power Estimation in Binary CMOS Circuits Based on Multiple-Valued Logic", OPA (Overseas Publishers Association) N.V., 2000.
5. Zhijin Guan, Wenjuan Li, Weiping Ding, Yueqin Hang (2011)"An Arithmetic Logic Unit Design Based on Reversible Logic Gates"978-1-4577-0253-2/11/$26.00 ©2011 IEEE.
6. C.H. Bennett, "Logical reversibility of Computation", IBM J.Research and Development, vol. 17(6), pp. 525–532, Nov. 1973.
7. Seema Rajput, Rita Jain and Awadhesh K. G. Kandu, "Review Of Full Adder Using Reversible Logic", International Journal of Electronics and Communication Engineering, Vol. 2(3), pp. 97-102, July 2013.
8. P. Kerntopf, "Synthesis of multipurpose reversible logic gates," in Proc. Euromicro Symp. DSD, pp. 259–267, 2002.
9. J. Lim, K. Kwon, and S. I. Chae, "Reversible energy recovery logic circuit without non-adiabatic energy loss," Electron. Lett., vol. 34(4), pp. 344–346, Feb. 1998.
10. Raghava Garipelly, P.Madhu Kiran, A.Santhosh Kumar, "A Review on Reversible Logic Gates and their Implementation", International Journal of Emerging Technology and Advanced Engineering, Vol. 3(3), pp. 417-423, March 2013.
11. P.Vanusha, K.Amurtha Vally, "Low Power Computing Logic Gates design using Reversible logic", Vol. 3(10), pp. 123-129, Oct. 2014.
12. Sk. Noor Mahammad and Kamakoti Veezhinathan, "Constructing Online Testable Circuits Using Reversible Logic", IEEE transactions on instrumentation and measurement, vol. 59(1), pp. 101-109, Jan. 2010.
13. D. Maslov and G. W. Dueck, "Garbage in reversible design of multiple output functions," in Proc. 6th Int. Symp. Represent. Methodology Future Comput. Technol., pp. 162–170, Mar. 2003.
14. P. Kerntopf, "Synthesis of multipurpose reversible logic gates," in Proc. Euromicro Symp. DSD, pp. 259–267, 2002.