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DESIGN OF CHANNEL LENGTH MODULATION FREE MOS TRANSISTOR

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Abstract

Recent days, MOS technology is dominating over BJT technology with its unique advantage of scaling towards lower technologies. This advantage is more suitable to design digital ICs with good accuracy in lower technologies. But, design of analog ICs in lower technologies with good accuracy is limiting due to the poor drain current versus drain-to-source voltage characteristics. These characteristics are deviating much compared with the ideal MOS characteristics due to finite channel length modulation. The prime aim is to minimize or eliminate this channel length modulation by designing suitable circuit techniques including MOS transistor, capacitor, resistor, diode etc. Once we can achieve these ideal characteristics of MOS Transistor, it opens an era to design analog and mixed signal ICs in lower technologies with good accuracy.

Keywords: Channel length modulation, MOS transistor, scaling, drain current, output resistance.

Introduction

One of the short channel effects in MOS transistors is Channel length Modulation, which is the major parameter that limits the ideal performance of MOSFET'S. It is due to the difference between drawn length and an effective length. Channel length modulation mainly occurs due to an increase in drain voltage, as drain voltage increases the drain depletion width tends to increase as drain and body junction is in reverse bias, which makes the effective channel length decrease when compared to drawn length. As a result the drain current increases which in turn reduces an output resistance. The output resistance of the MOS transistor can be increased in two ways, one is increasing the substrate doping density which is done at device level during fabrication process and the other is designing a circuit which consists of multiple MOS transistors and linear elements at the circuit level which mimics the exact behaviour of MOS transistor. As scaling increases towards the lower technology, the channel length modulation parameter increases. This effect

typically increases in small nano scale devices with low-doped substrates. This has become a major limitation in a MOSFET era. It can be overcome by proper scaling which can reduce channel length modulation parameter.

Proposed Two stage opamp design. On decreasing the gate length to nano level or even smaller, the gain of the circuits is reduced. We can overcome this by cascoding the transistors resulting in a high gain and good accuracy.

$$A_V = G_m.R_{out} = \frac{V_{out}}{V_{in}} \qquad (1)$$

The various ways to increase the gain of the circuit viz.. one among them is to increase the trans conductance (g_m) of the circuit and the other one is to increase the output resistance of the circuit.

$$\text{Trans conductance,} \quad g_m = \frac{I_{out}}{V_{gs}} \qquad (2)$$

Super 3t MOS: One of the easiest technique in super MOS transistors is Super 3t MOS. It consists of 3 transistors and an external current source. When super MOS is in saturation region, its characteristics are flat when compared to general NMOS which has bend in it. The improved super 3t MOS differs from super 3t MOS having a current mirror which allows the circuit to self bias as shown in Fig 2.

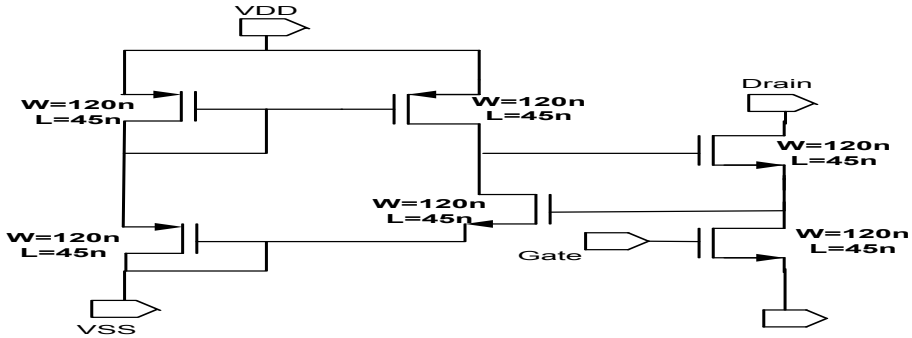


Fig.2 Schematic for Super 3t MOS.

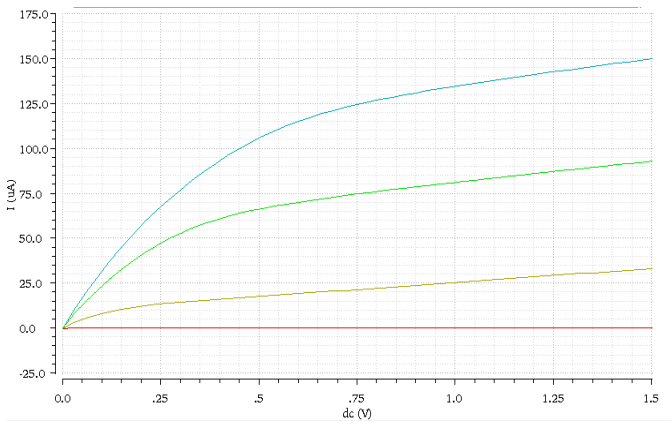


Fig.3 Simulation results of Super 3t MOS.

Super 13t MOS:

Super13t MOS transistors circuit as shown in Fig 4. This circuit mainly comprises of the combination of both PMOS and NMOS current mirrors. The main purpose of keeping this respective current mirrors are in order to acquire the same current with respect to both input as well as output of that particular part of the circuit. There are limitations of super 13t over super 3t MOS is increase in complexity, an increase in power consumption and an increase in area. The circuit as shown in Fig 4 consists of namely a biasing stage, a transresistance amplifier and a cascode output. Six transistors are connected to perform the operation of transresistance amplifier namely N_2, N_3, P_2, P_3, P_4, P_5. Transistor N_1 is current limiting factor for the drain current. The biasing of N_1 can be determined by the overdrive voltage of N_0.

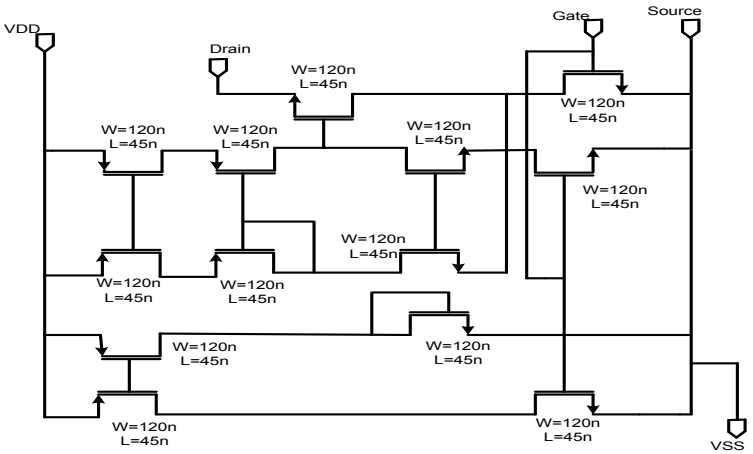


Fig. 4 Schematic of Super 13T MOS.

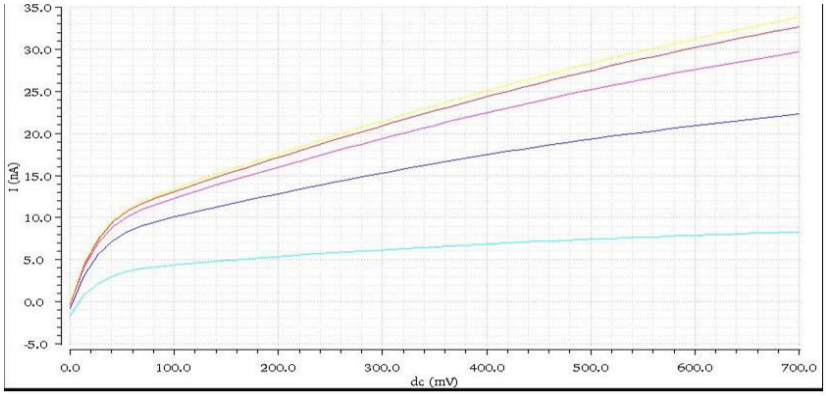
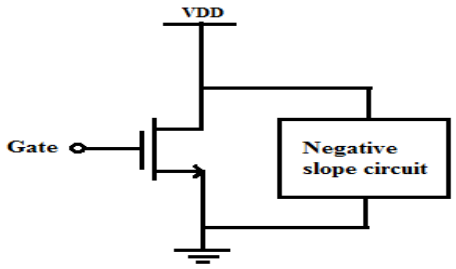


Fig. 5 Simulation results of Super 13T MOS.

III. Proposed Technique

The basic idea behind the proposed technique is to cancel the positive slope of drain current characteristic curve in saturation region by employing the circuit which induces negative slope. If we look at the MOS characteristics curve, we observe a positive slope which should have remained constant so as to minimize the parameter. By inducing a negative

slope curve in saturation region of MOS drain characteristics, it results in cancelling of positive and negative slope, resulting in a constant straight line.



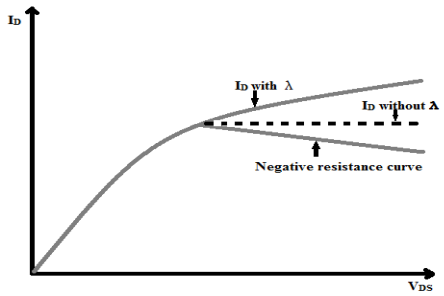


Fig.6 Proposed method. **Fig. 7 Characteristics of proposed method.**

Negative resistance MOS circuits:

A combination of MOS transistors and linear resistors can exhibit negative resistance. There are many circuits using MOS that can exhibit negative resistance. One such combination is NMOS cross coupled circuit which exhibit negative resistance of $-1/g_m$ which was shown in Fig 8.

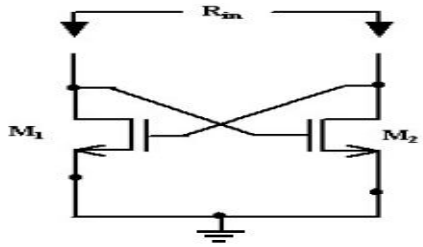


Fig. 8 NMOS cross coupled circuit.

R_{OUT}: Output impedance of MOS transistor by proposed technique.

r_{out} : Output impedance of normal MOS transistor.

g_m : Transconductance

IV. Schematic proposed technique:

In the proposed technique, MOS negative resistance circuit is connected across the drain terminal of normal MOS transistor (NM0). The drain current of NM0 MOS transistor is drawn by the negative resistance circuit. The resistance R0 and R3 are used for biasing the NM0 MOS transistor. All the MOS transistors in the negative resistance circuit are to be operated in saturation region. Three terminals are drawn out of the entire circuit which acts as drain, source and gate of the new implemented MOS transistor as shown in figure .9. This entire circuit will behave as a MOS transistor with reduced λ and increased output impedance.

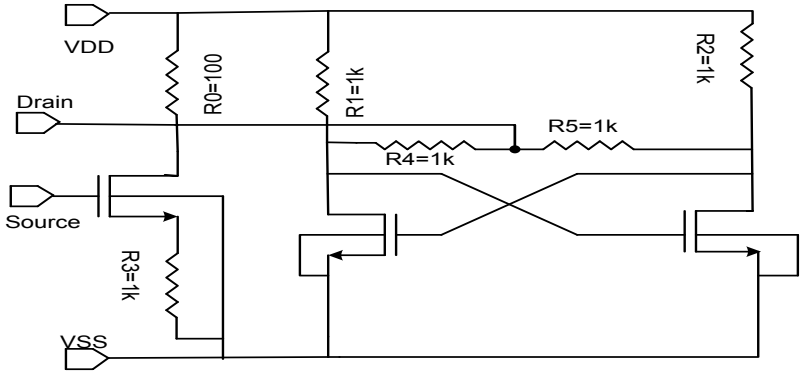


Fig.9 Schematic Slope cancelation technique.

IV. Simulation Results

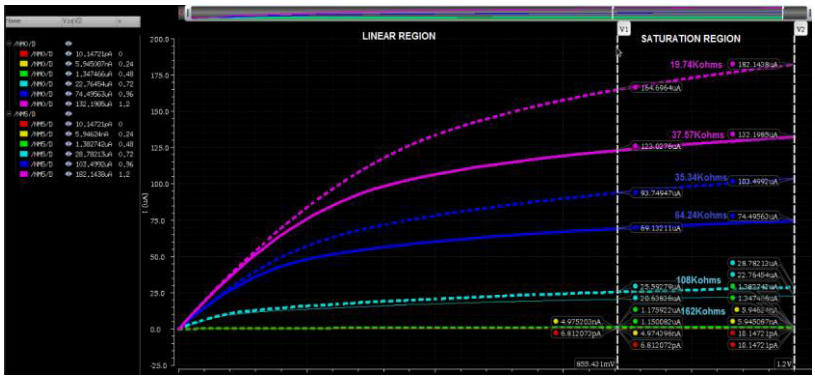


Table.1 Comparison Results at Vgs=0.6V

Parameter	Super 3T	Super 13T	Negative resistance circuit
λ in saturation	0.26 V^{-1}	0.12V^{-1}	0.03 V^{-1}
r_o in saturation	25.44kΩ	38.12kΩ	64.24kΩ

MOSFET is an incredible device which has opened a gateway to a new leading era and has wide number of applications when compared to BJT. One of the parameters affecting the ideal behavior of the MOSFET is channel length modulation parameter. Minimizing this parameter can make MOSFET to perform at its best performance. In this paper we have compared the characteristics of both super 3t and super 13t in terms of their output resistance and respective parameters as it is tabulated, which is not at all approximate to achieve the best characteristics of the MOSFET. Hence, through this paper we have introduced a new technique called the slope cancellation technique which may minimize the effect of channel length modulation parameter. If this approach has to be utilized in future, then it might be a great boon for circuit designers. The greatest advantage of using this method is to maximize the output resistance and to minimize the channel

length modulation parameter and ultimately achieved our target while designing a channel length modulation free MOS transistor.

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