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SIMULATION OF VECTOR CONTROLLED MULTILEVEL INVERTER FED INDUCTION MOTOR

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Abstract

This paper presents the simulation of vector control of multilevel inverter fed induction motor drive. The inverter harmonic content can be reduced by using multilevel inverter. In symmetrical circuit the voltage and power increases with the increase in level of inverter. Space Vector Modulation (SVM) technique is used to control the output of inverter. As power devices have been added in multilevel inverter structure, the voltage waveform has more redundant switching states, so that switching angle can be chosen for harmonic reduction. The model of the multilevel inverter system is developed with SVM strategy to control the induction motor. The speed and the flux are sensed for controlling the switching strategy thereby increasing the performance of multilevel inverter fed induction motor drive system.

1. Introduction

Power electronic inverters are becoming popular for various industrial drives applications. In recent years also high-power and medium-voltage drive applications have been installed [1], [2]. To overcome the limited semiconductor voltage and current ratings, some kind of series and/or parallel connection will be necessary. Due to their ability to synthesize waveforms with a better harmonic spectrum and attain higher voltages, multi-level inverters are receiving increasing attention in the past few years [3]–[6]. However, the increasing number of devices tends to reduce the overall reliability and efficiency of the power converter. On the other hand, solutions with a low number of devices either need a rather large and expensive LC output filter to limit the motor-winding insulation stress, or can only be used with motors that do withstand such stress. The performance of the multilevel inverter is better than classical inverter. The total harmonic distortion of the classical inverter is very high. In other words the total harmonic distortion for multilevel

inverter is low. The diode clamped inverter provides multiple voltage levels from a series bank of capacitors. The voltage across the switches is only half of the DC bus voltage. These features effectively double the power rating of voltage source inverter for given semiconductor device. In the present work an attempt is made to simulate vector controlled induction motor drive using Matlab Simulink.

The induction motor, which is the most widely used in the industry, has been favored because of its simple and rugged structure, low cost and reliability, etc. The concept of vector control has opened up a new possibility that induction motors can be controlled to achieve dynamic performance as good as that of DC motors. In order to understand and analyze vector control, the dynamic model of the induction motor is necessary. It has been found that the dynamic model equations developed on a rotating reference frame is better way to describe the characteristics of induction motors. Speed controlled induction motor drives are wide-spread electromechanical systems suitable for a large spectrum of industrial applications. When high dynamic performance and high precision control in a wide speed range are required, vector control of induction motor based on the availability of the speed sensor is used.

2. Voltage level notation

The switching states s_a , s_b and s_c will be defined for the *a*, *b* and *c* phase respectively. Each switching state has a range from 0 to (n-1) in order to represent the complete number of switching levels. Assuming proper operation, the inverter output line-to-ground voltages follow the switching states as,

$$\begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} = \left(\frac{v_{dc}}{n-1} \right) \begin{bmatrix} s_a \\ s_b \\ s_c \end{bmatrix} \qquad (1)$$

According to the modulation process, the output is an ideal sine-wave with switching harmonics. It is fairly obvious that increasing the inverter levels results in an inverter output voltage that more closely tracks the ideal sinusoidal output. The line-to-neutral voltages may be determined directly from the line-to-ground voltages by [4].

$$\begin{bmatrix} v_{an} \\ v_{bn} \\ v_{cn} \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} \qquad (2)$$

Inverter line-to-line voltages are related to the line-to-ground voltages by

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix} \quad (3)$$

Shows the switching state, line-to-ground voltage, line-to-neutral voltage, and line-to-line voltage for the case where n = 3. Therein, the line-to ground voltage contains a third harmonic component which is added in order to maximize the inverter output voltage [5]. Therein, it can be seen that the line-to neutral and line-to-line voltages do not contain the third harmonic. Also, it is interesting to note that these voltages contain more levels than the original line-to ground voltages. It is easily understood that there are 2n-1 line-to-line voltage levels consisting of *n* positive levels, *n* negative levels, and zero.

3. Voltage Vectors

It is required to view the voltages in the *q-d* stationary reference frame. The resulting vector plot contains information from all three phases and displays redundant switching states. The plot is particularly useful for comprehending the higher number of switching states [6]. The vector diagram has also been used to formulate multilevel modulation. However, it will be shown later that this is more readily accomplished in the time domain. The inverter voltages can be expressed in the arbitrary *q-d* reference frame by [13].

$$\begin{bmatrix} v_{qn} \\ v_{dn} \\ v_{0n} \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \sin(\theta) & \sin(\theta - \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) \\ 1/2 & 1/2 & 1/2 \end{bmatrix} \begin{bmatrix} v_{ag} \\ v_{bg} \\ v_{cg} \end{bmatrix}, \quad (4)$$

Considering (1), (2), and that the angle is θ=0 for the stationary reference frame, the *q-d* stationary voltages can be expressed in terms of the switching states by

$$v_{qn}^{s} = \frac{v_{dc}}{3(n-1)} \left(2s_a - s_b - s_c\right) \quad (5)$$

$$v_{dn}^{s} = \frac{v_{dc}}{\sqrt{3}(n-1)} \left(s_c - s_b\right) \quad (6)$$

The vector plot created by graphing the voltage vector defined by

$$v_{sw} = v_{qn}^{s} - jv_{dn}^{s} \quad (7)$$

for all possible switching states. Figure 3 shows the vector plot for the three level inverter. Therein, each vector and V_{sw} is denoted with a unique number. For the general *n* level inverter vector number can be related to the switching state by

$$sw = n^2 s_a + n s_b + s_c \qquad (8)$$

Figure 1 shows $sw = n_{sa}^2 + ns_b + s_c$ that there are several vectors, which result from a number of switching states. This switching state redundancy occurs since the common-mode component of the switching states is not included in the two-dimensional voltage vector plot. For the general *n*-level three-phase inverter, there are

$$n_{sw} = n^3 \qquad (9)$$

Switching states and

$$n_{vec} = 3n\,(n-1) + 1 \qquad (10)$$

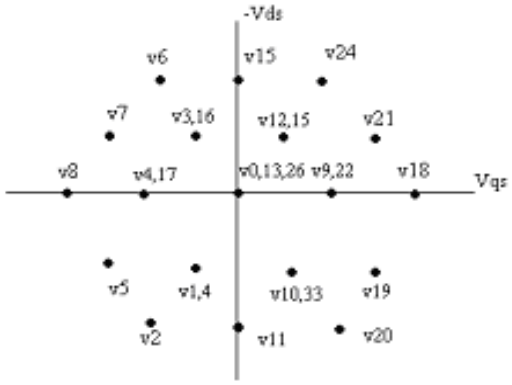

Fig.1 Voltage vector.

4. Multilevel inverter

The diode-clamped inverter provides multiple voltage levels through connection of the phases to a series bank of capacitors. According to the original invention [2], the concept can be extended to any number of levels by increasing the number of capacitors. Early descriptions of this topology were limited to three-levels [3] where two capacitors are connected across the dc bus resulting in one additional level. The additional level was the neutral point of the dc bus, so the terminology neutral point clamped inverter was introduced [3]. However, with an even number of voltage levels, the neutral point is not accessible, and the term multiple point clamped is sometimes applied [4]. Due to capacitor voltage balancing issues, the diode-clamped inverter implementation has been mostly limited to the three level. Figure 2 shows the topology of the three-level diode-clamped inverter. Although the structure is more complicated than the two-level

inverter, the operation is straightforward and well known [4]. Each phase node (*a*, *b*, or *c*) can be connected to any node in the capacitor bank (d_0, d_1, or d_2). Connection of the *a*-phase to junctions d_0 and d_2 can be accomplished by switching transistors T_{a1} and T_{a2} both off or both on respectively. These states are the same as the two-level inverter yielding a line-to-ground voltage of zero or the dc voltage. Connection to the junction *d1* is accomplished by gating T_{a1} off and T_{a2} on. In this representation, the labels T_{a1} and T_{a2} are used to identify the transistors as well as the transistor logic (1=on and 0=off). In a practical implementation, some dead time is inserted between the transistor signals and their complements meaning that both transistors in a complementary pair may be switched off for a small amount of time during a transition [9]. From Figure 2 it can be seen that, with this switching state, the *a*-phase current and i_{as} will flow into the junction through diode D_{a1} if it is negative or out of the junction through diode D_{a2} if the current is positive. According to this description, the inverter relationships for the *a*-phase are presented in Table 1.

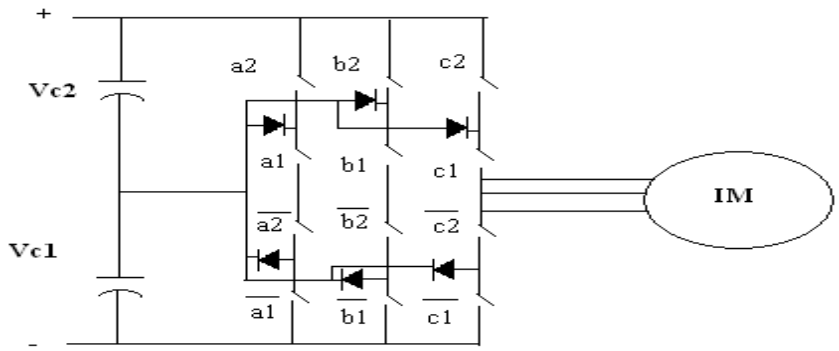

Fig.2 Three level inverter.

If each capacitor is charged to one-half of the dc voltage, then the line-to-ground voltage can be calculated by the ideal equation (1). The dc currents i_{abc1} and i_{abc2} are the *a*-phase components to the junction currents i_{abc1} and i_{abc2} respectively.. In the literature [1] to [10] the frequency spectrum and speed response of three level inverter fed induction motor is not presented. In the present work an attempt is made to obtain the frequency spectrum and speed response of three phase induction motor drive system.

Table 1: Three-level inverter relationships

S_a	a2	a1	ν_{ag}	i_{1adc}	i_{2adc}
0	0	0	0	0	0
1	0	1	ν_{c1}	i_{as}	0
2	1	1	$\nu_{c1} + \nu_{c2}$	0	i_{as}

4. Space Vector Modulation

Space vector modulation (SVM) is based on vector selection in the *q-d* stationary reference frame. As an example, consider the commanded voltage vector defined for a three-level system, the commanded vector is plotted along with the vectors obtainable by the inverter in Figure 1.

The desired vector v_{qds}^{S*} is shown at some point in time, but will follow the circular path if a three-phase set of voltages are required on the load. Although the circular path shown in the figure, the path may be arbitrary. The first step in the SVM scheme is to identify the three nearest vectors. In this example, they are v_{52} , v_{56} and the redundant vectors v_{36} & v_{57} . The next step is to determine the amount of time that must be spent at each vector in order for the average voltage to be equal to the commanded voltage. This can be done using some simple mathematical relationships. In particular, the vectors and their corresponding times are related by

$$v_{35,46} T_{35;46} + v_{41}, T_{41} + v_{45}, T_{45} = v_{qds}^{s*} T_{sw} \qquad (11)$$

where *sw T* is the switching time of the SVM control which is the total of the time spent at each vector or

$$T_{sw} = T_{36,57} + T_{52} + T_{56} \qquad (12)$$

Based on (11) and (12), the amount of time for each voltage vector can be computed by solving the inverse problem

$$\begin{bmatrix} \mathrm{Re}\{v_{36,57}\} & \mathrm{Re}\{v_{52}\} & \mathrm{Re}\{v_{56}\} \\ \mathrm{Im}\{v_{36,57}\} & \mathrm{Im}\{v_{52}\} & \mathrm{Im}\{v_{56}\} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} T_{36,57} \\ T_{52} \\ T_{56} \end{bmatrix} = \begin{bmatrix} \mathrm{Re}\{v_{qds}^{s*}\} \\ \mathrm{Im}\{v_{qds}^{s*}\} \\ T_{sw} \end{bmatrix} \quad (13)$$

The final step in the SVM scheme is to determine a sequence of switching for the Voltage vectors and corresponding output voltage.

6. Vector control

The aim of vector controlled induction motor drive is to obtain the characteristic of a DC motor using induction motor. It can be obtained by using parks and inverse parks transformation blocks. The simulink model for vector controlled induction motor system is shown in figure 3.

The scope is connected to measure parameters like voltage, rotor speed and torque. The pulses are generated using SVM method. The speed loop ensures that the actual speed of the motor is equal to set speed. The current loop provides protection for the devices in the inverter.

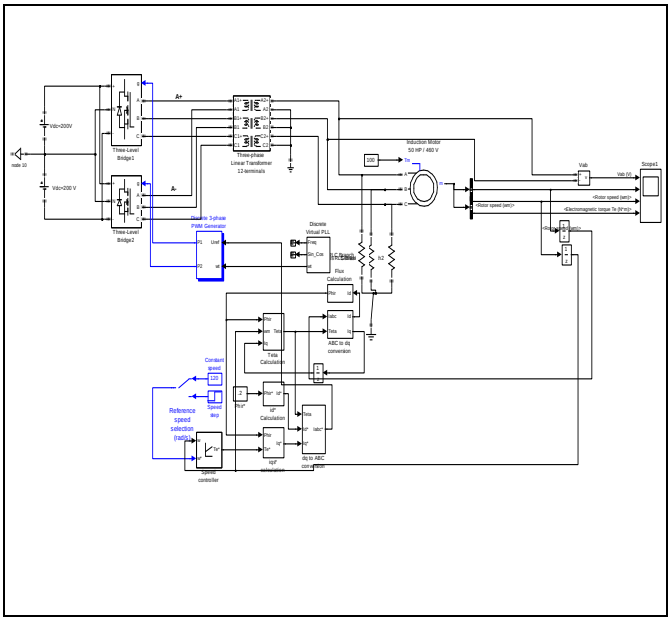

Fig. 3. Simulink model for vector controlled drive.

7. Simulation Results

The simulation studies have been done on a three level inverter fed 5 HP induction motor rated 460 Volts, 60 Hz, 1750 RPM. The line to line voltage is shown in figure 4. The rotor speed variation is shown in figure 5 and the electromagnetic torque variation is shown in figure 6. The rotor speed reaches the set value as shown in figure5. From the torque waveform it can be seen that the torque ripple is reduced in steady state.

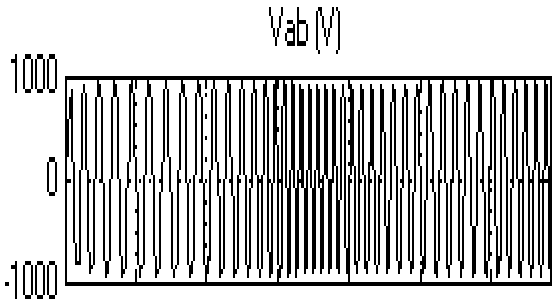

Figure. 3. Line Voltage.

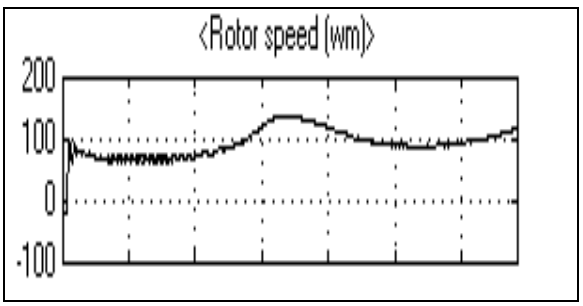

Fig. 4. Rotor speed.

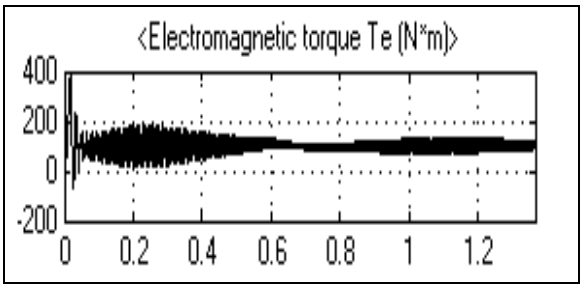

Fig. 5. Electromagnetic torque.

8. Conclusion

The vector controlled multilevel inverter fed induction motor drive is simulated using Matlab Simulink. The multilevel inverter output has reduced harmonics. This reduces the heating of stator winding of the induction motor. The torque of the motor can be controlled by controlling the quadrature axis component current. The speed can be controlled by controlling the direct axis component current. From the simulation results it is observed that the vector controlled induction motor has characteristic similar to that of DC motor. The simulation results are similar to the theoretical results.

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