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COMPARISON OF A NOVEL 15 LEVEL CASCADED ASYMMETRIC MULTICELL INVERTER USING PI AND FUZZY LOGIC CONTROLLER

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Abstract

This paper proposes a 15 level cascaded asymmetric multicell converter. With this new topology of inverter a cell consists of a dc source and two switches. The asymmetric DC sources are binary in progression. By cascading of the cells are capale of producing positive voltage levels which in turn called as auxiliary inverter. The output of auxiliary inverter is fed into main inverter to produce positive and negative output voltage levels (AC output voltage). Another noteworthy feature of this topology is that if any H-bridge fails, it can be bypassed and the configuration can still operate as a five level inverter at its full power rating. The Multi carrier based Level shifting Phase Disposition Pulse width Modulation (LS-PD-PWM) technique is involved to reduce the percentage of distortion. This paper also compares the performance analysis of the circuit by using Proportional Integral (PI) and Fuzzy Logic Controller which is used to produce reference signal for LS-PD-PWM. The complete system is modeled and simulated in MATLAB/SIMULINK environment. The results are obtained from proposed circuit shows that the circuit works properly to produce the multilevel output with low total harmonic distortion using the controllers. Simulation results show the effectiveness of the proposed topology of switching.

Keywords: Cascaded H- bridge multilevel inverter, Level shifting Phase Disposition Pulse width Modulation (LS-PD-PWM), Proportional Integral (PI)

1. Introduction

The recent trend to meet an ever-increasing energy demand is moving toward generating power with renewable energy source that may be dispersed in a wide area, and most of them are renewable, as they have greater advantages due to their environmentally friendly nature. Cascaded H bridge multilevel inverters overcome the disadvantages of conventional two level inverter through combining two H-bridge module together because of its level increasing

ability. An advanced configuration for symmetric multilevel voltage source inverter is proposed it can able to generate the desired voltage levels using a lower number of circuit devices including power semi-conductor switches and related gate driver circuits of switches [1]. A developed cascaded multilevel inverter is comprised of series connection in order to generate all voltage levels even and odd at the output[2].Proposed VSI that has been designed to reduce circuit complexity by optimizing the use of bidirectional switches is built by adding an auxiliary circuit comprising an arrangement of bidirectional switches to the three-phase, six-switch, full-bridge configuration.[3]. A new topology proposed and require a less number of dc voltage source and less semiconductor devices consists of lower blocking voltage on switch, that results in decreased complexity[4].Recently, a novel MVSI has been suggested, that is reduced the power components [5]. A redundant switching state for generating different pole voltages proposed by selecting appropriate switching states, and if any H bridge fails, it can be by passed and this configuration works in three level inverter [6].Fuzzy logic controller is implemented for shunt APF, to compensate reactive power and to eliminate harmonics drawn from a diode rectifier feeding RL load during distorted voltage conditions [7]. Proposed PD modulation scheme on series converters that may applied to parallel converters using interleaving techniques with multilevel characteristics [8]. A novel topology proposed for medium voltage applications, this converter linking series connected half bridge module at each phase that can be extended to large portion [9].New topology with a reversing voltage component is shown to improve performance by compensating some disadvantage like complex PWM and voltage balancing problem in conventional inverters is proposed [10]. An effective hybrid optimal modulation technique is proposed for cascaded H-bridge inverter with generalized optimal pulse width modulation can be extended to m-level [11]. An alternative way of improving the control performance a classic digitally controlled power converter with multisampling techniques is proposed here which can posses the advantage of reducing switching delay [12]. Hybrid inverter stages with high, medium and low voltage is made to reduce dc source, a novelty control method is presented to avoid undesirable high switching frequency for high and medium stages of inverter [13].A study of novel five level multistring inverter topology is proposed with front end stage to improve the conversion efficiency of conventional boost converters for PV application [14].A five level multistring inverter for PV grid connected system is proposed with novel PWM technique, two reference signal that are identical to each other with offset [15]. A new integrated fuzzy logic controller modulator is proposed with new power sharing algorithm for cascade H bridge multilevel inverters for efficiency issues in interactions between stages [16].A stable current output adjusting modulation index for multilevel inverter with fuzzy logic controller has

developed for variable speed wind turbine system [17].A comparison is made with relations between space vector modulation and carrier based pulse with modulation with vector calculations [18].This opens a space for embarking on research work in designing and illustrating the a newly constructed simplified three phase cascade H bridge multi level inverter topology with level shifting phase disposition pulse width modulation and comparison is made with PWM, PI controller and fuzzy logic controller[19].

2. Proposed Cascaded Multicell Inverter.

A cascade multilevel inverter consists many number of H-bridge (single-phase full bridge) inverter connected in cascaded fashion.. The proposed cascaded multi cell multilevel inverter is a mixed version of cascaded and flying capacitor multi cell inverter. Here the positive switch and the negative switch were connected to the dc source which we call as cell. These cells are connected in cascaded fashion to produce the output levels. Then these voltages are fed through normal single phase inverter o produce the positive and negative voltage levels[20]. The circuit is shown in Figure 10.

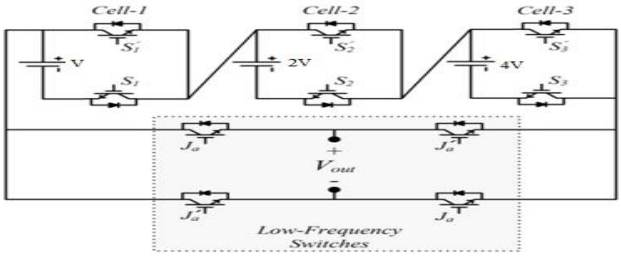


Figure 1.Structure of Proposed Cascaded H-Bridge multi cell MLI.

In the proposed 15 level inverter we have three cells connected in cascaded fashion. The cell 1 has two switches S_1 and S_1'. The switch S1 is called positive switch used to produce positive voltage and the switch S_1' is called negative switch used to produce negative voltage[21].

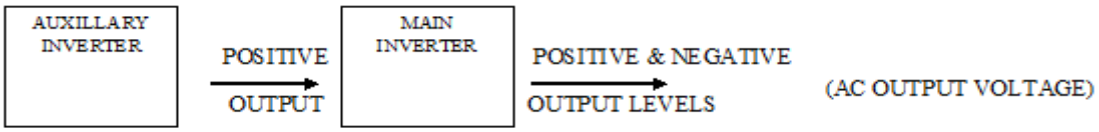


Figure 2. Working of Proposed Cascaded H-Bridge multi cell MLI.

Here we use asymmetric dc voltages whose voltage levels are given as V for cell 1, 2V for cell 2, 4V for cell 3 etc. Each H-bridge has separate dc source. Each DC source is associated with one single-phase full-bridge inverter[22]. The output voltages of each cell are connected in series in order to produce multilevel output at the inverters. Their peak to peak voltage available is the addition of all the voltage sources. In our case the peak to peak voltage is 7V. Here, we used voltage of about 40V. So we produce the output voltage of about 280V. The operation is similar to that

of the cascaded H-Bridge inverter. Each cell produces output levels of +V , -V and Zero volts. The comparison between conventional and proposed inverter is shown in Table 2.

A fifteen -level cascaded converter, for example, consists of three DC sources and three full bridge converters. The switching pattern to produce 15 voltage levels is shown in the Table 1.

The relation between the no of output levels and no of semiconductor devices are calculated by using the formulae as shown below[23]. Let us calculate the no of devices used in each phase where "N_{DC}" be the number of DC sources or stages and the associated number of output voltage level can be calculated by using the equation[24],

$$M = 2^{Ndc} \qquad (1)$$

The number of switches used in this topology for auxillary inverter is given by the equation,

$$N_S = 2(N_{DC}) \qquad (2)$$

The number of switches used in this topology for main inverter is given by the equation,

$$N_{SMAIN} = 4 \qquad (3)$$

Therefore the total no of switches used in each phase is

$$N_{TOTAL} = N_s + NS_{MAIN}$$

$$N_{TOTAL} = 2(N_{DC}) + 4 \qquad (4)$$

Where,

M = No of output voltage levels

N_S = No of switching devices in auxiliary inverter

N_{SMAIN} = No of switching devices in main inverter

N_{TOTAL} = Total no of switching devices.

Table– 1. Switching table for 15-level asymmetrical Cascaded multicell converter.

Output voltage levels	**Auxillary switches**		**Main switches**					
	J_a	**J_a'**	**S_1**	**S_2**	**S_3**	**S_1'**	**S_2'**	**S_3'**
7V	ON	OFF	ON	ON	ON	OFF	OFF	OFF
6V	ON	OFF	ON	ON	OFF	OFF	OFF	ON
5V	ON	OFF	ON	OFF	ON	OFF	ON	OFF
4V	ON	OFF	ON	OFF	OFF	OFF	ON	ON
3V	ON	OFF	OFF	ON	ON	ON	OFF	OFF
2V	ON	OFF	OFF	ON	OFF	ON	OFF	ON
1V	ON	OFF	OFF	OFF	ON	ON	ON	OFF
0	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
-1V	OFF	ON	ON	ON	OFF	OFF	OFF	ON
-2V	OFF	ON	ON	OFF	ON	OFF	ON	OFF
-3V	OFF	ON	ON	OFF	OFF	OFF	ON	ON
-4V	OFF	ON	OFF	ON	ON	ON	OFF	OFF
-5V	OFF	ON	OFF	ON	OFF	ON	OFF	ON
-6V	OFF	ON	OFF	OFF	ON	ON	ON	OFF
-7V	OFF	ON	OFF	OFF	OFF	ON	ON	ON

Table– 2. Comparison of Cascaded H-Bridge and Proposed MLI.

Output Voltage Levels	Cascade H-Bridge		Proposed cascade H -Bridge	
	Single phase	Three phase	Single phase	Three phase
	Number of switches used	Number of switches used	Number of switches used	Number of switches used
	(2*(m-1)	3*(2*(m-1)	(m+1)	3*(m+1)
9	16	48	8	24
15	28	84	10	30
31	60	180	12	36

3. Modulation Techniques

The power electronic components IGBT MOSFET JFET etc., are operated in the "switched mode" which means the switches are always in either one of the two states - turned off (cutoff region), or turned on (saturated region with only a small voltage drop across the switch). Any transition from conducting to non-conducting causes unwanted signals to flow through them. To control the flow of power in the circuits, the switches alternate between these two states (i.e. on and off). The switched component is attenuated and the desired DC or low frequency AC component is retained. This process is called Pulse Width Modulation (PWM), since the desired average value is controlled by modulating the width of the pulses[25].

3.1 Classification of Modulation Strategies:

The purpose of the modulation technique of the multilevel inverter is to synthesize the output voltage nearest to that of the sinusoidal waveform. Many modulation techniques have been developed for harmonic reduction and switching loss minimization based on switching frequency[26].

3.2 Multicarrier Pulse Width Modulation:

Particularly for Multilevel inverters the Multicarrier PWM is easy to generate switching signals and also the output waveform appears as close as to the sinusoidal one.

There are off two types.

1. Phase Shifting PWM 2. Level shifting PWM

In PS-PWM techniques the carriers are equal in amplitude and frequency but they have phase difference with each other. In LS-PWM techniques the carriers are equal in amplitude, frequency and phase but they differ in their levels.

3.3 Level shifted PWM Method:

There are three alternative PWM strategies with different phase relationships for the level-shifted multicarrier modulation:

- Phase disposition (PD), where all carrier waveforms are in phase.

- Phase opposition disposition (POD), where all carrier waveforms above zero reference are in phase and are 180 degree out of phase with those below zero.
- Alternate phase disposition (APOD), where every carrier waveform is in out of phase with its neighbor carrier by 180 degree.

3.4 Phase Disposition (PD):

In the present work, in the carrier-based implementation the phase disposition PWM scheme is used. Generally the sinusoidal reference signal is compared with the triangular carriers to produce switching signals to the circuit. In the carrier-based implementation, at every instant of time the modulation signals are compared with the carrier and depending on which is greater, the switching pulses are generated (figure 3).

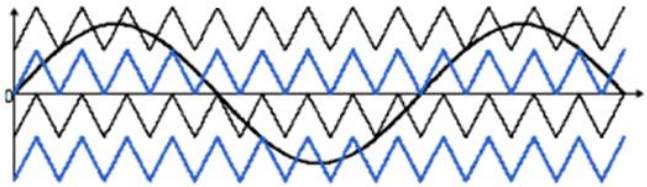


Figure 3. Level Shifting Phase Disposition Pulse Width Modulation (LS-PD-PWM).

In the similar way for an N –level inverter, the (N-1) triangles are used as carriers. The positive switches S1 and S4 uses the carrier above the zero biasing to produce the output voltages Vs/2 and Vs and the negative switches S2 and S3 uses the carriers below the zero biasing to produce the output voltages –Vs/2 and –Vs.

4. Control Strategy

4.1 Proportional integral controller

The Proportional Integral controller is a basic solution for most industrial applications. It is popular because of its simple structure and can be easily implemented in practice (figure 4). The control action law of a PI controller is defined by the following equation:

$$u(t) = K_p e(t) + K_i \int_0^t e(t)dt \qquad (5)$$

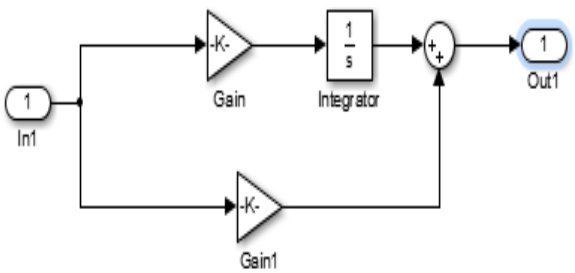


Figure 4. Implementation of PI controller.

4.2 Fuzzy logic controller

A Fuzzy Logic Controller (FLC) is basically designed by selecting its inputs and outputs, choosing the preprocessing needed for the inputs and de post – processing needed for the outputs, as well as designing each of its four basic components: Fuzzification, rule – base, inference mechanism and defuzzification (figure 10).

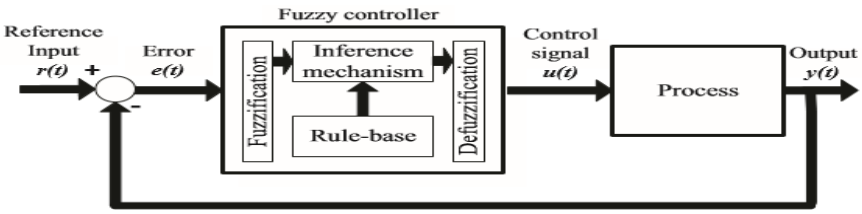
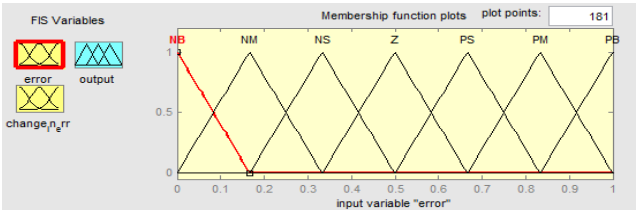


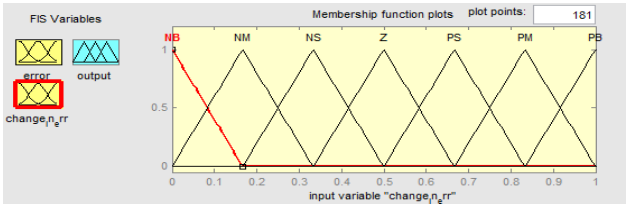
Figure 5.An FLC is an artificial decision making system that operates in closed loop and real time as can be observed.

4.3 Fuzzification

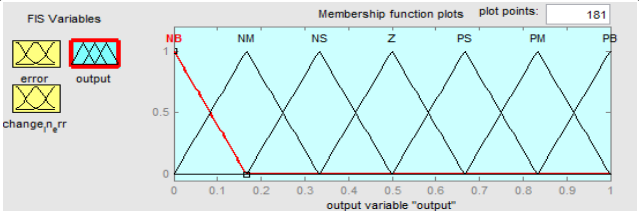
The membership function values are assigned to the linguistic variables using seven fuzzy subset called negative big (nb), negative medium (nm), negative small (ns), zero(z), positive small (ps), positive medium (pm), positive big (pb). Variable e and Δe are selected as the input variables, where e is the error and Δe is the change in error. The output variable is the reference signal for PWM generator (figure 6). Triangular membership functions are selected for all these process. Fuzzy associative memory for the proposed system is given in Table-3.



(a)



(b)



(c)

Figure 6. Membership Function Plot of Error , (b) Membership Function Plot of changein Error, (c) Membership Function Plot of output.

Table 3. Fuzzy Associate Memory for the Proposed System.

e	Δe						
	nb	nm	ns	zr	ps	pm	pb
nb	nb	nb	nb	nm	nm	ns	zr
nm	nb	nb	nm	nm	ns	zr	ps
ns	nb	nm	nm	ns	zr	ps	pm
zr	nm	nm	ns	zr	ps	pm	pm
ps	nm	ns	zr	ps	pm	pm	pb
pm	ns	zr	ps	pm	pm	pb	pb
pb	zr	ps	pm	pm	pb	pb	pb

5. Simulation and Experimental validations.

5.1 Output Voltage of 15 level Cascaded Multicell Inverter Using PWM Generator.

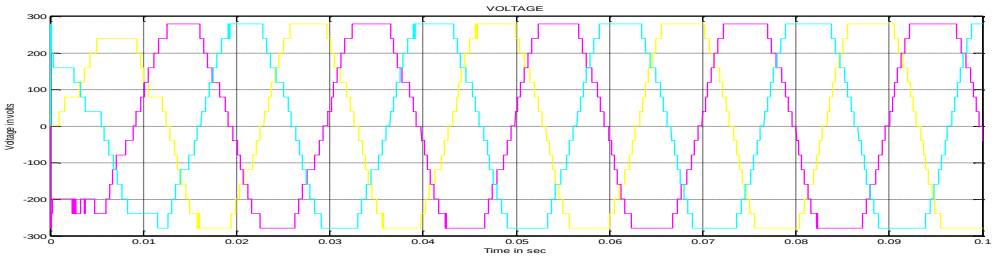


Figure 7. Obtained voltage waveform using PWM generator.

5.2 Output current waveform of 15 level Cascaded Multicell Inverter Using PWM Generator.

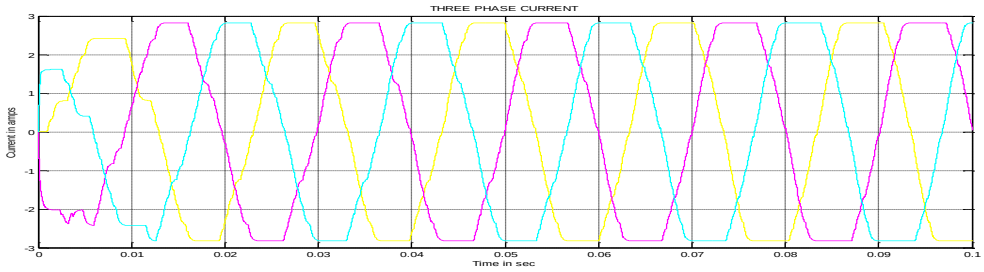


Figure 8. Obtained current waveform using PWM generator

5.3 THD of 15 level Cascaded Multicell Inverter Using PWM Generator.

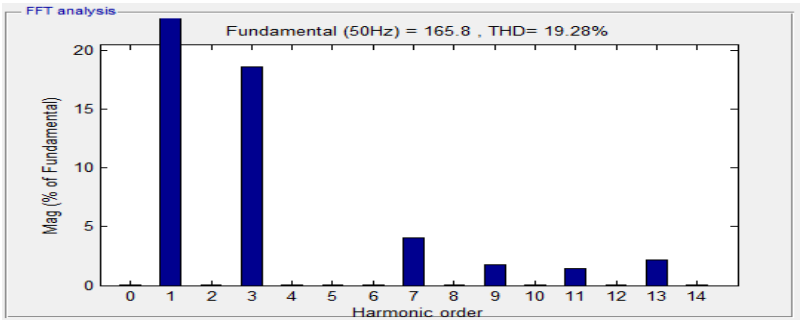


Figure 9. Total Harmonic Distortion of 15 level Cascaded Multicell Inverter Using PWM Generator.

5.4 Control Strategy of 15 level Cascaded Multicell Inverter Using LS-PD-PWM.

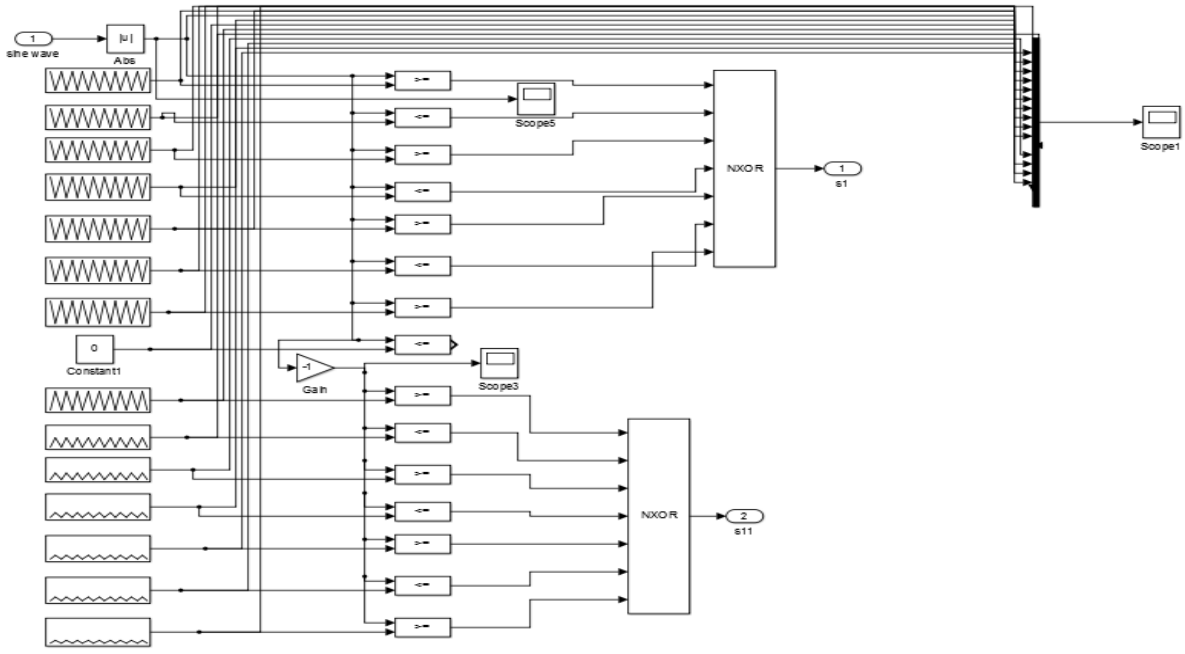


Figure 10. Control StrategyUsing LS-PD-PWM.

5.5 Carrier Arrangement using LS-PD-PWM

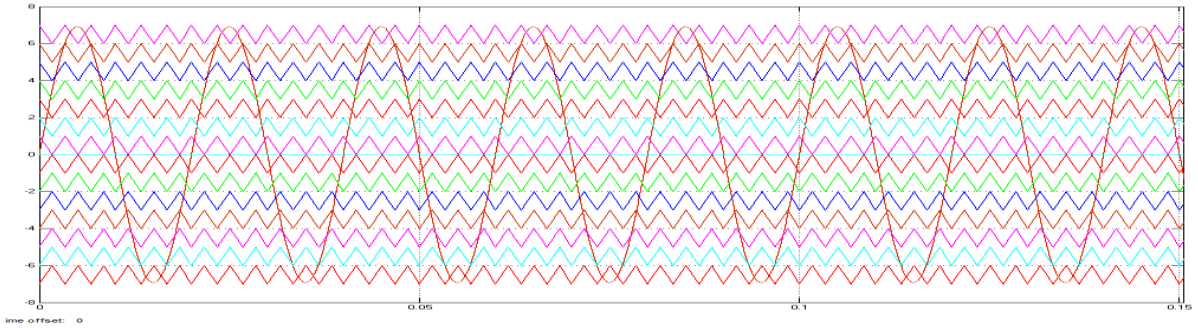


Figure 11. Carrier arrangement Using LS-PD-PWM.

5.6 Three Phase Output Voltage Of 15 level Cascaded Multicell Inverter Using LS-PD-PWM.

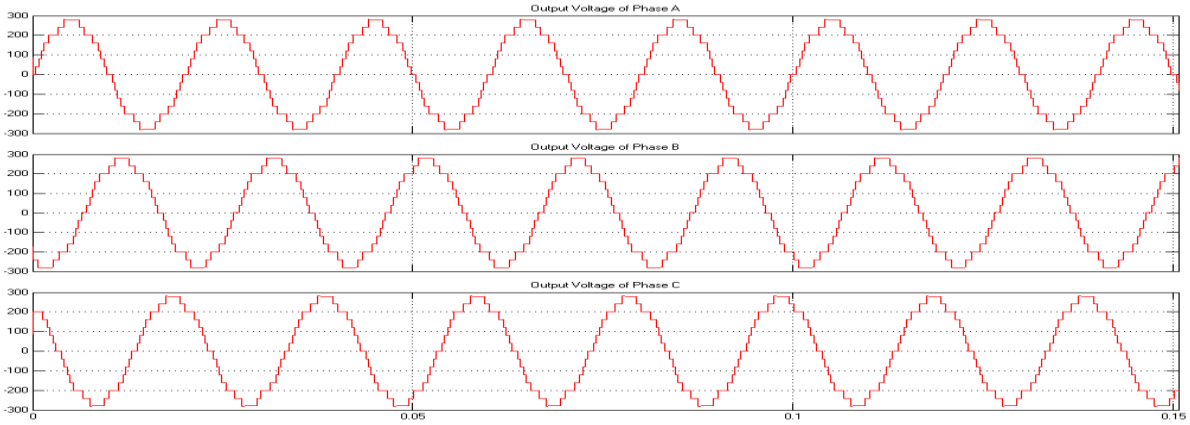


Figure 12.Obtained voltage waveform using LS-PD-PWM.

5.7 Three Phase Output Current Of 15 level Cascaded Multicell Inverter Using LS-PD-PWM.

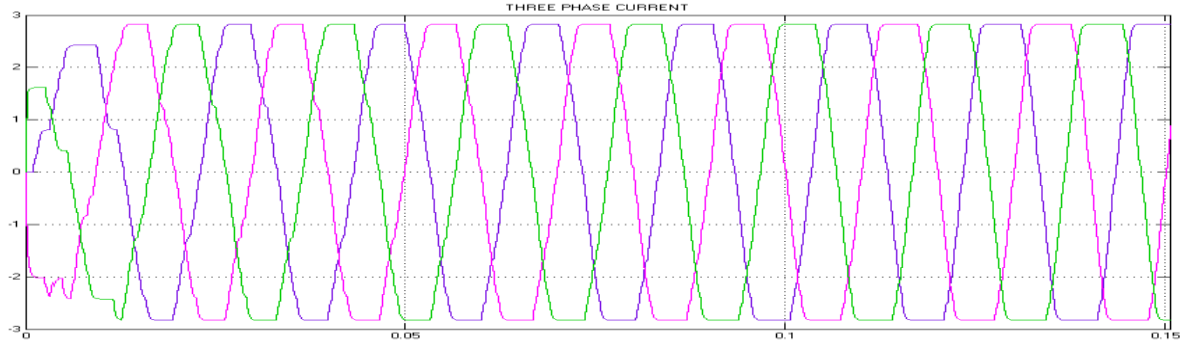


Figure 13.Obtained voltage waveform using LS-PD-PWM.

5.8 THD of 15 level Cascaded Multicell Inverter Using LS-PD-PWM.

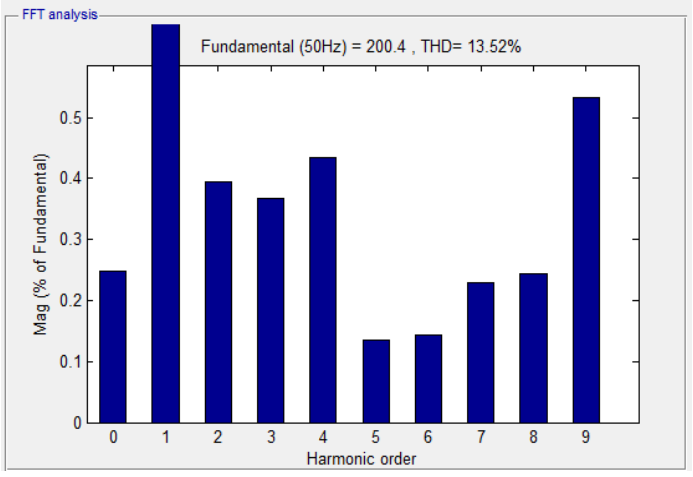


Figure 14. Obtained Total Harmonic Distortion of 15 level Cascaded Multicell Inverter Using LS-PD-PWM.

5.9 Control Strategy of 15 level Cascaded Multicell Inverter Using LS-PD-PWM Inverter with PI Controller

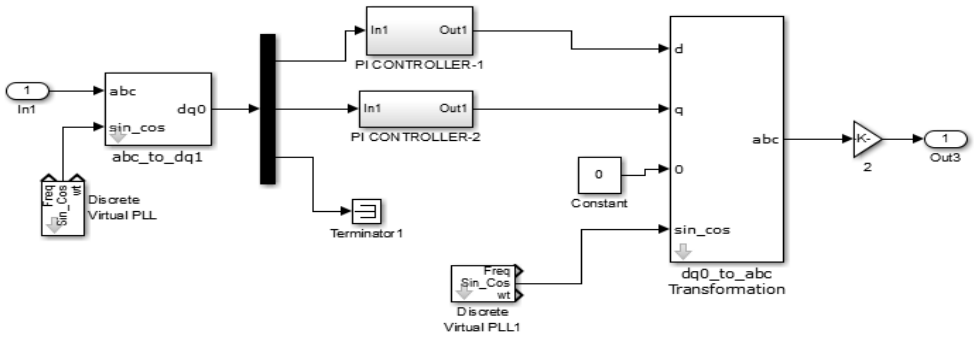


Figure 15. Control Strategy Using LS-PD-PWM.

5.10 Three Phase Output Voltage of 15 level Cascaded Multicell Inverter Using LS-PD-PWM with PI Controller.

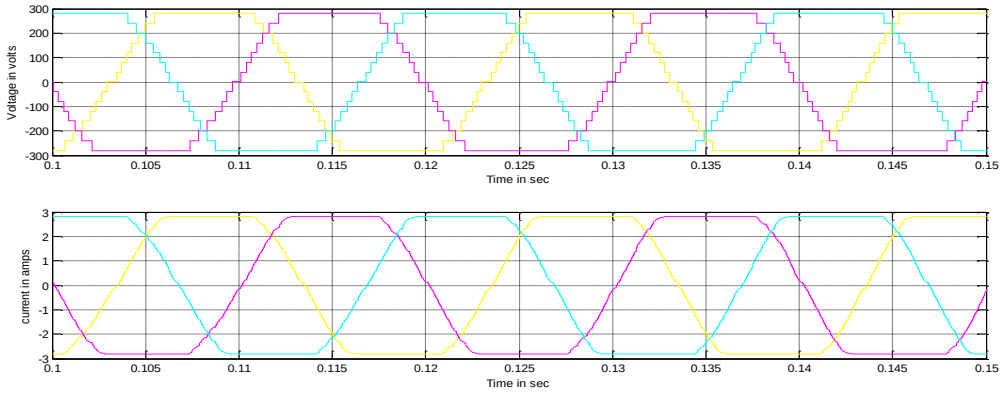


Figure 16.Obtained voltage and current waveform using LS-PD-PWM with PI Controller.

5.11 THD of 15 level Cascaded Multicell Inverter Using LS-PD-PWM with PI Controller.

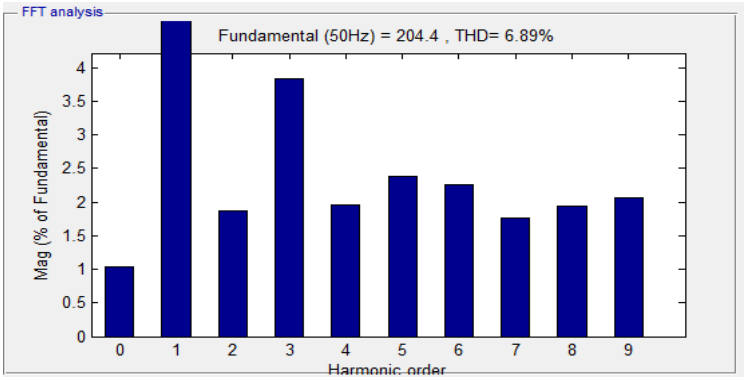


Figure 17. Obtained Total Harmonic Distortion of 15 level Cascaded Multicell Inverter Using LS-PD-PWM

5.12 Control Strategy of 15 level Cascaded Multicell Inverter Using LS-PD-PWM Inverter With Fuzzy Logic Controller.

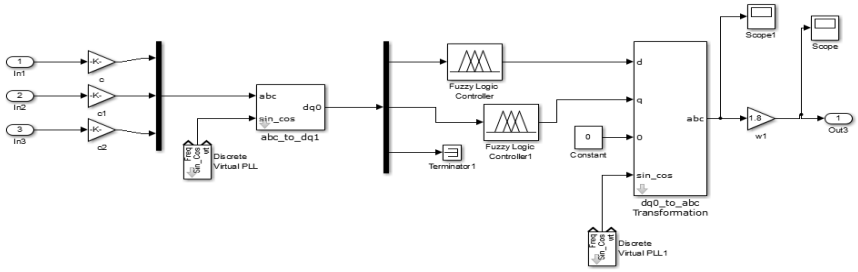


Figure 18. Control Strategy Using LS-PD-PWM with Fuzzy Logic Controller.

5.13 Fuzzy Rules

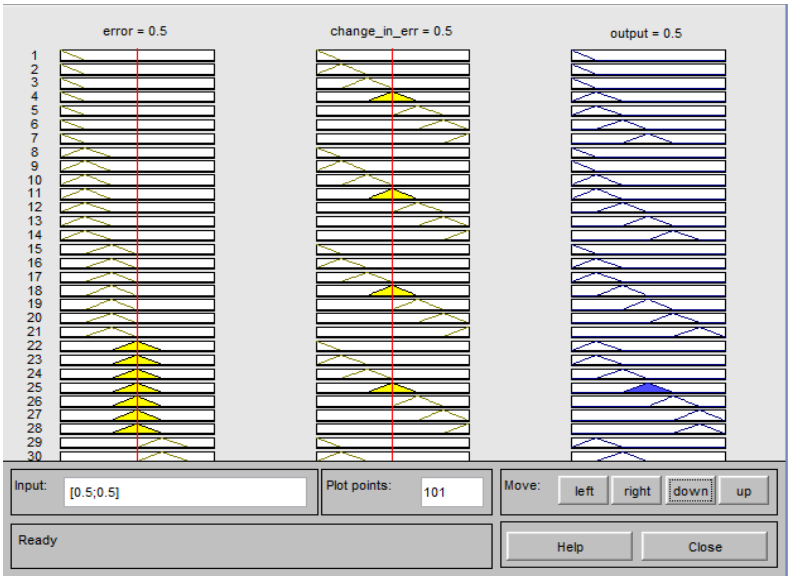


Figure 19. Implemented Fuzzy Rules for the Proposed System.

5.14 Fuzzy Structure

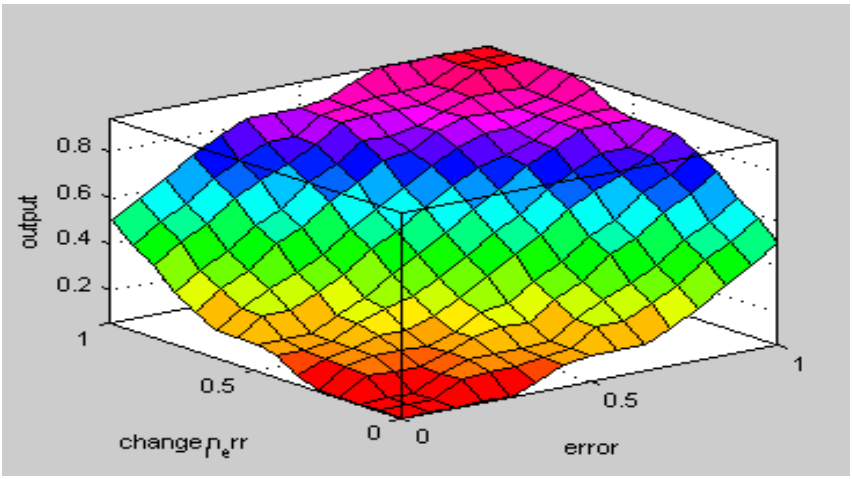


Figure 20. Obtained Fuzzy Structure

5.15 Three Phase Output Voltage of 15 level Cascaded Multicell Inverter Using LS-PD-PWM with Fuzzy Logic Controller

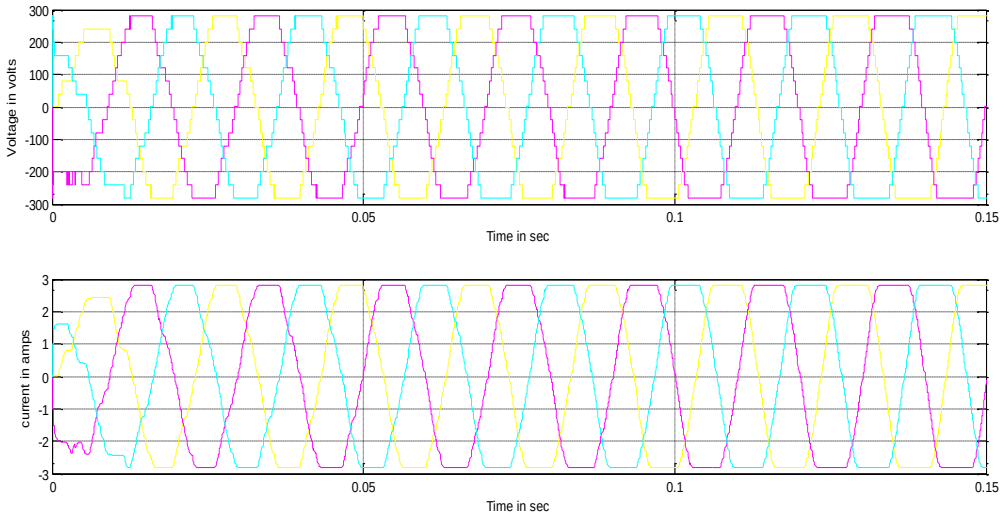


Figure 21. Obtained voltage and current waveform using LS-PD-PWMwith Fuzzy Logic Controller

5.16 THD of Nine Level Cascaded H Bridge Inverter Using LS-PD-PWMwith Fuzzy Logic Controller

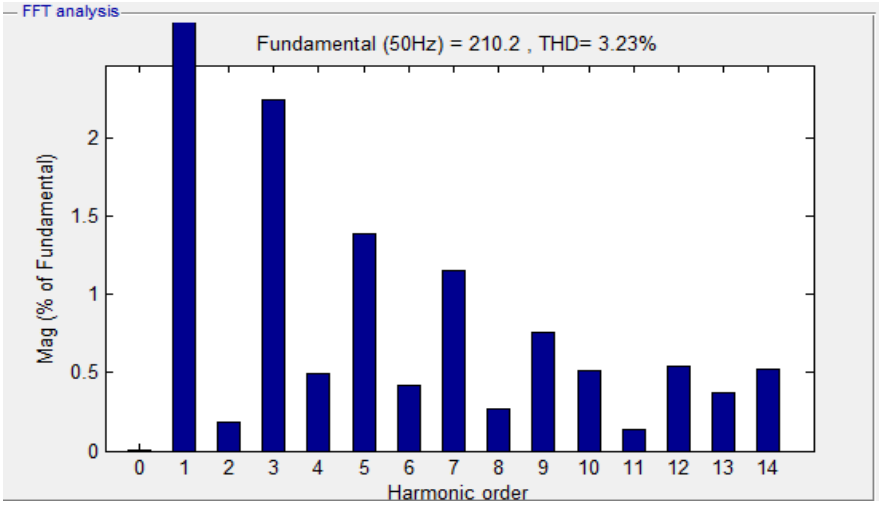


Figure 22. Obtained Total Harmonic Distortion of Nine Level Cascaded H Bridge Inverter with Fuzzy Logic Controller

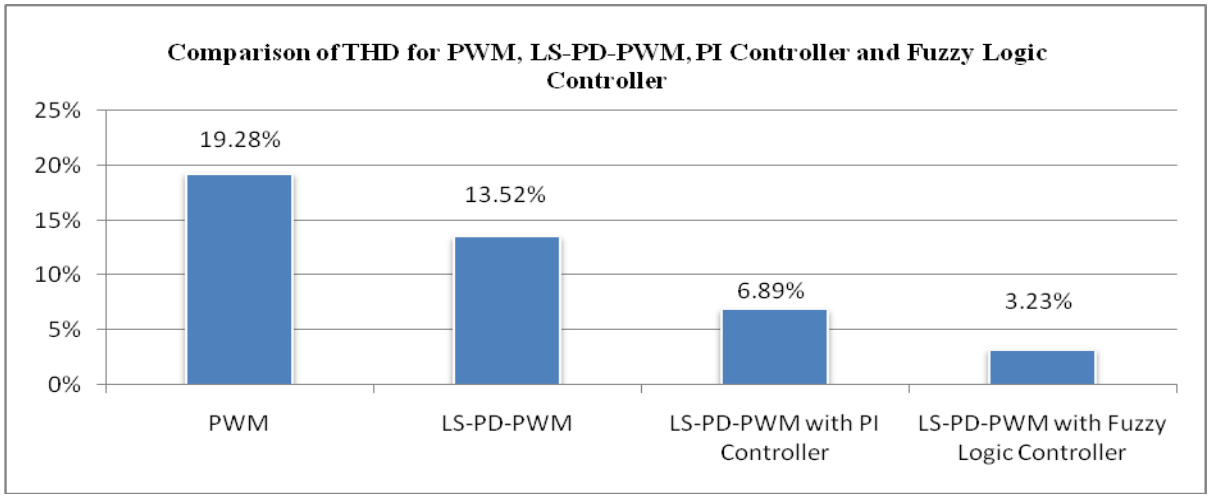


Figure 23. Comparison of THD for PWM, PI Controller and Fuzzy Logic Controller.

Conclusion:

This paper proposed new topology of cascaded asymmetric multicell inverter to produce multilevel output with significant reduction of power electronics components. The LS-PD-PWM technique involved to further improve the performance of the inverter by reduces the THD which was illustrated in figure 23. The simulation also proves that if any failure occurs in any one of the cell it can able to produce up to multiple voltage levels without shunt downing the entire systems.

The multilevel inverter was successfully controlled by both PI and fuzzy logic controller and these are used to achieve control of multilevel output steps both in linear and nonlinear loads. This paper also compares the performance of PI and Fuzzy logic controller. The simulation reveals that the Fuzzy logic controller is most efficient and effective than PI controller in our case. The simulation result also proves the effectiveness of the proposed switching topology.

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