ISSN: 0975-766X
CODEN: IJPTFI
Available Online through *Research Article*
www.ijptonline.com

A MODIFIED STRUCTURE OF CARRY SELECT ADDER USING CNTFET TECHNOLOGY

Karunakaran.P*[1], Dr.Sundarajan.M[2]
[1]Research Scholar, Bharath Institute of Higher Education and Research, Bharath University, Chennai-73.
[2] Principal, Sri Lakshmi Ammal Engineering College, Chennai.
Email: karunakaranvkp@gmail.com

Received on 10-07-2016 *Accepted on 25-08-2016*

Abstract

Carry Select Adder (CSLA) is one of the fastest adders used in many data processing processors to perform fast arithmetic functions. This work uses a simple and efficient gate level modification to significantly reduce the area and power of the CSLA. The modified design has reduced area and power as compared with multiternary digit (trit) adder design. The adder is based on an efficient single-trit full-adder design with low-complexity encoder and reduced complexity carry generation unit. Further, we optimize the number of encoder and decoder blocks required while putting together several single-trit full-adder units to realize a multitrit adder. Extensive HSPICE simulation results show roughly 79% reduction in power-delay product for three-trit adders and 88% reduction in power-delay product for nine-trit adders in comparison to a direct realization.

I. Introduction

Design of area- and power-efficient high-speed data path logic systems are one of the most substantial areas of research in VLSI system design. In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The sum for each bit position in an elementary adder is generated sequentially only after the. Previous bit position has been summed and a carry propagated into the next position. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum [1]. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input Cin=0 and Cin=1, then the final sum and carry are selected by the multiplexers (mux).The basic idea of this work is to use Binary to Excess-1

Converter (BEC) instead of RCA with Cin=1 in the regular CSLA to achieve lower area and power consumption [2]–[4]. The main advantage of this BEC logic comes from the lesser number of logic gates than the n-bit.

Full Adder (FA) structure. The details of the BEC logic are discussed in Section III.

New technologies include the carbon nanotube field effect transistor (CNTFET), single electron transistor, silicon-on-insulator, and fin-field effect transistor. Among these, CNTFET is promising in view of ballistic transport and low OFF-current properties enabling high-performance and low power design [5]–[11]. This letter presents efficient designs of 1) a single-ternary digit (trit) adder and 2) a multitrit adder in CNTFET. Ternary logic is specifically chosen for the design since it has an elegant association with CNTFET. In particular, CNTFETs provide the possibility of realizing two distinct threshold voltages merely by the use of different diameters of the carbon nanotube [12]. Further, ternary logic achieves simplicity and energy efficiency in digital design since it reduces the complexity of interconnects and chip area. For example, 14-bit binary addition can be done (roughly) by a nine-trit adder.

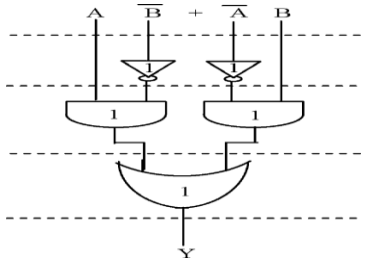


Fig.1. Delay and Area Evaluation an XOR gate.

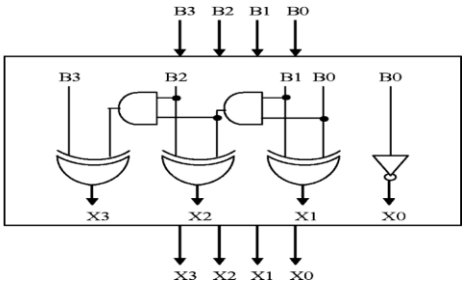


Fig.2. 4-Bit BEC.

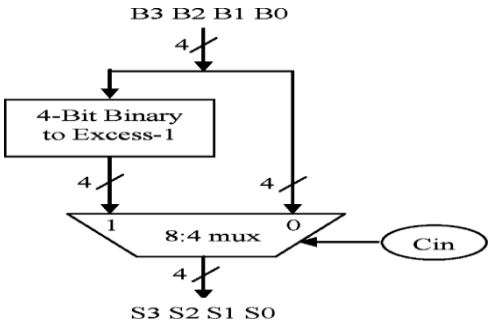


Fig.3. 4-Bit BEC with 8:4 mux.

II. Single-Trit Adder

Our single digit adder solution is based on a small modification of the ternary decoder in [6]. This leads to a lower complexity half adder as well as full-adder. We focus on the full-adder here since it constitutes the building block of the multidigit adder. The general structure of a one-trit adder with three ternary inputs *A,B,* and *C*in and two ternary outputs *C*out and Sum as shown in Fig. 1. It turns out that the encoder and carry-generation unit in Fig. 1 can be improved upon (when compared with prior designs in [8] and [6]). The proposed modification of the decoder (in [6]) is shown in Fig. 2. The ternary NOR gate of [6] is replaced here by a binary NOR since the inputs are Boolean. Also, complements of *A*0 and *A*2 are obtained with merely one inverter. While the circuit for *sum-generate* in Fig. 4 is the same as prior designs, the proposed *carry-generate* circuit requires fewer gates (as discussed later). Let the output carry of the *carry-generate* block in Fig. 4 when encoded be denoted by *CXo* and *CY o*. Then, *CX o* and *CYo* are given as: *CXo* = _(*A,B,Ci*) =

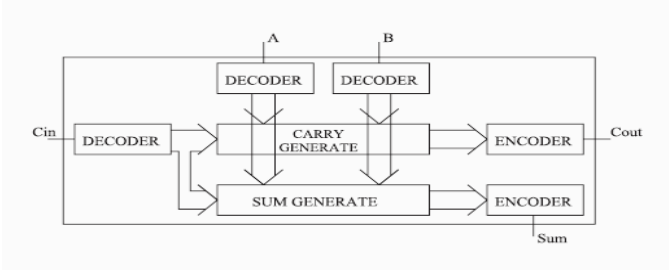


Fig.4. Ternary full adder Block Diagram.

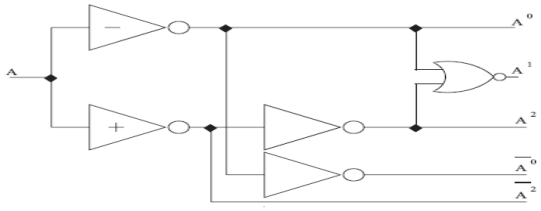
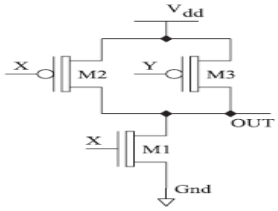


Fig.5. Decoder



X	Y	OUT	Voltage value
0	0	2	V_{dd}
0	2	2	V_{dd}
2	0	1	$V_{dd}/2$
2	2	0	0

$\overline{(2,2,2)}$. $C_o^Y = \Pi(A,B,C_i) = \Pi\{(0,0,0),(0,1,0),(0,2,0),(1,0,0),(1,1,0),(2,0,0),(0,0,1),(0,1,1),(1,0,1),(0,0,2),(2,2,2)\}$. The simplified expressions for C_o^X and C_o^Y are given by

$$C_o^X = \overline{A^2} + \overline{B^2} + \overline{C_i^2}$$
$$C_o^Y = (A^0 + \overline{B^2})(\overline{A^2} + B^0)(\overline{A^2} + C_i^0)(\overline{B^2} + C_i^0)$$
$$(A^0 + B^0 + C_i^0)(A^0 + \overline{C_i^2})(B^0 + \overline{C_i^2}). \quad (1)$$

Fig.6. Proposed.

Encoder

It is worth noting that *CXo* as well as *CYo* are independent of *A*1, *B*1, and *C*1*i*. This has valuable consequences: the propagation to the next stage (especially for realizing a multitrit adder) becomes easier without *encoder–decoder* pairs (additional details are provided in Section III). Equation (1) suggests that the carries can be realized using only eight binary AND gates, one binary NAND gate, and one binary NOR gate. The availability of *A*2, *B*2, and *C*2 *i* via the modified decoder facilitates low-complexity carry generation.

*Remark 1: A*0 output of the decoder is used in the derivation of equations of sum. The equations for sum are omitted since carry propagation is the key to multidigit adder design.

Remark 2: Dhande and Ingole [8] present a half-adder architecture that uses three ternary AND and one ternary OR (besides a *T*-buffer) for carry generation. The design in [6] realizes the carry using three binary AND and one binary OR (besides a *T*-buffer). The direct extension of the design in [6] to the full adder requires 11 binary AND gates and 1 binary OR gate .With respect to the encoder in Fig. 1, the proposed design and its truth table are given in Fig. 3. Note that only three transistors are required here while a *T*-buffer followed by a ternary-OR gate are used in the design in [6]. Additional data in support of the savings are provided in Table II.

TABLE I
REQUIRED DECODER OUTPUT FOR DIRECT PROPAGATION OF CARRY

Output	Encoder inputs		Actual outputs of Decoder			Required outputs of Decoder	
Z	E_1^X	E_0^X	D^2	D^1	D^0	D_0^Y	D_1^Y
0	2	2	0	0	2	2	2
1	2	0	0	2	0	2	0
2	0	0	2	0	0	0	0

IV. Proposed Multitrit Adder in Cntfet

Fig. 5 forms the basis for the design of an efficient multitrit adder. Consider the two-trit adder in Fig. 4 which is a direct extension of the one-trit adder of Fig. 5.In Fig. 7, the signal "X," which is two-digit valued has output carry information of first stage but in Boolean format. However, signal "Y," which is the decoded signal of first stage carry output is three-digit (three-valued). Therefore, signal "X" cannot be propagated to the next stage without conversion back to ternary. Since the encoder is simplified as shown in Fig. 6, if the decoder is designed to get "X" and "Y" in Fig. 7 exactly the same, the block shown by _1 can be removed from the circuit leading to the reduction in overall propagation delay. To facilitate this, we construct Table I and study what is required by the decoder. It is clear from Table I that there are simple relations between the required decoder outputs and actual decoder outputs.

In particular, $D2 = DY0$,$D1 = \text{NOR}(DY0, DY1)$, and $D0 \; DY1$ .Therefore, the actual decoder outputs can be evaluated directly from the encoder inputs without using the block shown by_1 in Fig. 7. Only "00" combination is considered as inputs of encoder for logic "2" output (instead of both "00" and "02" shown in Fig. 6) to avoid confusion with respect to the actual decoder outputs. The outputs at each stage, denoted by $C2i$ and $C0i$, resemble the first stage carry CXo and CYo. In particular, the output carry signals $C2o$ and $C0o$ become $C21$ and $C01$ for the first stage, $C22$ and $C02$for the second stage and so on. Therefore, the carry signals of ith stage are given by (2). The circuit realizing

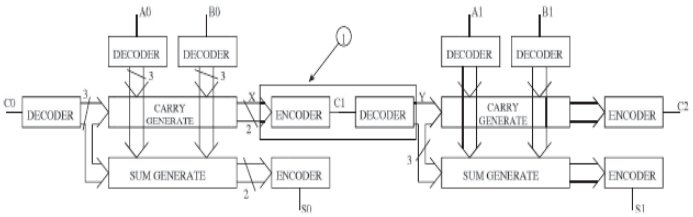


Fig.7. Two –trit Adder.

The realization of a multitrit adder incorporating these ideas is given in Fig. 6. BLOCK A and BLOCK C are direct implementations of carry expressions and their duals, respectively, of a full adder whereas LOCK B is for other unary signals ($A1$, $B1$, and $C1i$) followed by the implementation of sum expressions of a full adder.

Remark 3: In the proposed encoder (see Fig. 3), there exists a path between Vdd and ground for an input combination of $\{X = 2, Y = 0\}$ leading to an output voltage of Vd d 2 and power consumption in standby mode due to static current (which becomes significant for multitrit adders). This problem can be mitigated using power gating. In this approach, we connect an additional high-threshold voltage NMOS-CNTFET between ground and the source of the existing NMOS-CNTFET in the encoder .

TABLE II
COMPARISON OF SINGLE-DIGIT TERNARY FULL ADDERS

Adder type/ Parameter	Circuit of [6]	Proposed Ternary Adder
Worst-case Delay (τ) in ps	73.27	50.77
Average Power in μW	35.94	23.77
PDP in 10^{-15}J	1.72	0.85

V. Stimulation Result

In this section, we present the results of HSPICE simulation using the MOSFET-like CNTFET model at 0.9 V power supply and room temperature. The transient response of the proposed one-trit adder is designed. The propagation delays have been measured from change in input to possible transitions of sum and carry outputs., $t$sum−1 , $t$sum−2 , $t$sum−3 ,

*t*sum−4 , *t*sum−5 , and *t*sum−6 are the transition delays from the change in input (*A*, *B*, or *Ci*) to change in sum output for "0→1," "1→2," "2→0," "0→2," "2→1," and "1→0" transitions, respectively. Similarly, *t*carry−1 , *t*carry−2 , *t*carry−3 , and *t*carry−4 are the delays from the change in input (*A*, *B*, or *Ci*) to change in carry output for "0→1," "1→2," "2→1," and "1→0," transitions, respectively. (It is worth noting that the transitions of carry output given by "2→0" and "0→2" are not possible for a single-input transition.) From the transient response, we can infer the following: *t*sum−1 = 44.165 ps, *t*sum−2 = 39.874 ps, *t*sum−3 = 50.77 ps, *t*sum−4 = 34.202 ps, *t*sum−5 = 30.068 ps, *t*sum−6 =47.238 ps, *t*carry−1 =37.129 ps, *t*carry−2 =32.636 ps, *t*carry−3 =9.238 ps, *t*carry−4 =32.510 ps. The simulation results are presented in Table II. The PDP is the product of average delay and average power consumption.

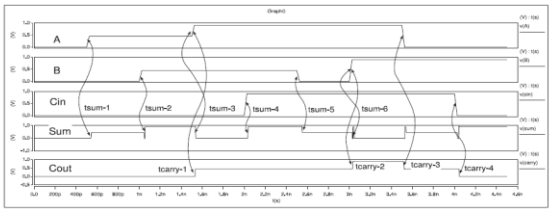


TABLE III
COMPARISON OF THREE-TRIT AND NINE-TRIT ADDERS

Parameter/ Adder type	Worst-case Delay (τ) in ps	Avg. Power in μW	PDP in f J
3-trit adder using 1-trit adder in [6]	187	43.1	5.44
3-trit adder using proposed 1-trit adder	66.17	23.1	1.09

Fig.8. Transient response of the proposed ternary full adder

Table III presents the results for the proposed multitrit adders (and in particular for three-trit and nine-trit adders). Since no multitrit adders are available to our knowledge, we have also implemented a direct realization of three-trit and nine-trit adders based on the designs of the one-trit adder. *f*J in Table III refers to 10−15 J.

VI. Conclusion

New designs for single-trit and multitrit adders in CNTFET are presented. It is worth noting that the transistor-based design approach (as opposed to gate-level design) adopted for encoder as well as carry generation leads to an efficient solution. The proposed designs achieve low power-delay product.

References

1. O. J. Bedrij, "Carry-select adder," *IRE Trans. Electron. Comput.*, pp. 340–344, 1962.
2. B. Ramkumar, H.M. Kittur, and P. M. Kannan, "ASIC implementation of modified faster carry save adder," *Eur. J. Sci. Res.*, vol. 42, no. 1, pp. 53–58, 2010.

3. T. Y. Ceiang and M. J. Hsiao, "Carry-select adder using single ripple carry adder," *Electron. Lett.*, vol. 34, no. 22, pp. 2101–2103, Oct. 1998.
4. Y. Kim and L.-S. Kim, "64-bit carry-select adder with reduced area," *Electron. Lett.*, vol. 37, no. 10, pp. 614–615, May 2001.
5. A. Rahman, J. Guo, S. Datta, and M. Lundstrom, "Theory of ballistic nanotransistors," *IEEE Trans. Electron. Devices*, vol. 50, no. 10, pp. 1853– 1864, Sep. 2003.
6. Y. Lin, J. Appenzeller, J. Knoch, and P. Avouris, "High-performance carbon nanotube field effect transistor with tunable polarities," *IEEE Trans Nanotechnol.*, vol. 4, no. 5, pp. 418–489, Sep. 2005.
7. I. O'Connor, J. Liu, F. Gaffiot, F. Pregaldiny, C. Lallemant, C. Maneux, J. Goguet, S. Fregonese, T. Zimmer, L. Anghel, T. Dang, and R. Leveugle, "CNTFETmodeling and reconfigurable logic-circuit design," *IEEE Trans. Circuits Syst.-I*, vol. 54, no. 11, pp. 2365–2379, Nov. 2007.
8. A. Akturk, G. Pennington, N. Goldsman, and A. Wickenden, "Electron transport and velocity oscillations in a carbon nanotube," *IEEE Trans. Nanotechnol.*, vol. 6, no. 4, pp. 469–474, Jul. 2007.
9. J. G. Delgado-Frias, Z. Zhang, and M. Turi, "Low power SRAM cell design for FinFET and CNTFET technologies," in *Proc. IEEE Int. Green Comput. Conf.*, Aug. 2010, pp. 547–553.
10. S. Lin, Y.-B. Kim, and F. Lombardi, "CNTFET-based design of ternary logic gates and arithmetic circuits," *IEEE Trans. Nanotechnol.*, vol. 10, no. 2, pp. 217–225, Mar. 2011.
11. A. Raychowdhury and K. Roy, "Carbon-nanotube-based voltage-mode multiple-valued logic design," *IEEE Trans. Nanotechnol.*, vol. 4, no. 2, pp. 168–179, Mar. 2005.
12. A. P. Dhande and V. T. Ingole, "Design and implementation of 2-bit ternary ALU slice," in *Proc. Int. Conf. IEEE-Sci. Electron. Technol. Inf. Telecommun.*, Mar. 2005, pp. 17–21.
13. T. Yamada, "Analysis of submicron carbon nanotube field-effect transistors," *Appl. Phys. Lett.*, vol. 76, no. 5, pp. 628–630, Jan. 2000.
14. S. Heinze, J. Tersoff, R. Martel,V. Derycke, J. Appenzeller, and P.Avouris, "Carbon nanotubes as Schottky barrier transistors," *Phys. Rev. Lett.*, vol. 89, no. 10, pp. 106 801-1–106 801-4, Sep. 2002.

Corresponding Author:

Karunakaran.P*,