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A STUDY ON VARIOUS ISSUES IN VLSI LOW POWER TESTING

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Abstract:

In present era VLSI testing, very high power consumption is sizably voluminous issue. It is withal the most astronomically immense concern for today's SoC, while diminishing the configuration endeavors, utilization of IP cores in SoC has further hyperbolized the high power consumption during testing. This paper contains the detailed survey on sundry power reduction techniques for testing like external testing, and internal testing like Built-In Self-Test techniques (BIST), DFT techniques.

Key Words: Built-In Self-Test techniques (**BIST**), Design for Testing (**DFT**), Automatic Test Pattern Generation (**ATPG)** algorithms, Automatic Test Equipment (**ATE**), Linear Feedback Shift Register (**LFSR).**

1. Introduction:

The high power consumption is a sizably voluminous challenge to both design and test engineers. [1].Reducing the power consumption during mundane function mode further expanded the power consumption quandary during test. Commonly, a circuit may deplete more power in the test mode than in the mundane mode. In order to avoid that, the semiconductor industry is probing for low-power testing techniques [2]. To decrease the expense and time to market, utilization of IP core is to a great extent received for SoC. Power lessening amid testing of such cores puts numerous requirements on current low-power testing strategies.

2. High-Power utilization amid test:

This segment depicts the purpose behind high-power utilization amid test. There are a few explanations behind high test power. The principle reasons are, in the test mode, the switching activity of all nodes is few times higher than the switching activity amid typical operation. In a SoC, parallel testing is much of the time performed to diminish the test

time, which might build power and energy dissipation. Input vector applied to a given circuit has critical relationship amid system mode, while the successive test patterns have very low correlation. This prompts larger switching activity and power dissipation in circuit amid test than during its ordinary operation. To reduce the test complex difficulty, the design-for-testability circuitry is deeply set surrounded by and part of circuit. It is generally useless during typical operations however might be seriously utilized as a part of the test mode.

3. Influences of High power dispersal amid testing:

Very high-power dissipation during test causes an IC to fall flat. Because of the electro relocation circuit can be fizzled. Need of at-rate testing can be restrictioned as a result of high-power dissipation. Stuck at fault can be tried effortlessly, however the testing of the delay fault will get to be troublesome. The impact of test power dissipation can produce lifted test warm that requires more costly package or it cause lasting harm to the circuit under test (CUT). The high test power dissipation causes expansive voltage drop that leads the circuit to glitch in test mode just and subsequently prompt yield misfortune. Amid utilitarian testing of the die after wafer etching, the unloaded uncovered die gives next to no sum power or heat dissipation [3] this might be an issue for multichip module innovation.

4. Models of energy and power:

Power utilization in CMOS circuits can be grouped into static and dynamic. Dynamic power dissipation is created by switching activities of the circuits. A higher operating frequency prompts more regular switching activities in the circuits and results in expanded power dissipation. Static power dissipation is identified to the logical states of the circuits as opposed to switching activities.

In CMOS logic, leakage current is the main wellspring of static power dissipation. However, occasional deviations from the strict CMOS style logic can bring about static current to be drawn. The most critical wellspring of dynamic power dissipation in CMOS circuits is the charging and discharging of capacitance. Sometimes, capacitors are purposefully created to accomplish certain non-digital operations, for example, charge sharing and signal delay. However, most digital CMOS circuits do not require capacitors for their planned operations. The capacitance shapes because of parasitic impacts of interconnection wires and transistors. Such parasitic capacitance can't be stayed away from and it significantly affects the power dissipation of the circuits.

- Amid the charging cycle, the energy E_s drawn from the voltage source is,

$$E_s=C_LV^2 \longrightarrow (1)$$

Where E_s is the energy drawn from the voltage source, C_L is the load capacitance.

- The energy put away in the capacitor toward the end of the charging cycle is

$$E_{cap}=1/2C_LV^2 \longrightarrow (2)$$

E_{cap} is the energy put away in the capacitor.

- The energy E_c dissipated during charging is,

$$E_c = E_s - E_{cap} = 1/2C_LV^2 \longrightarrow (3)$$

- Presently consider the discharging cycle, we expect the capacitor is completely discharged the energy E_d dissipated amid discharge cycle,

$$E_d=1/2C_LV^2 \longrightarrow (4)$$

E_d is precisely equivalent to the energy put away in the capacitance toward the start of the discharging cycle.

- If we charge and discharge the capacitance at the frequency of f cycles per seconds,the power dissipation of the system is

$$P = E_s f = C_LV^2f \longrightarrow (5)$$

- The aggregate power ought to be summed over every capacitance C_i in a circuit

$$P = \sum_i C_iV^2 f_i \longrightarrow (6)$$

Where V_i is the voltage swing across the capacitor C_i switching at frequency f_i.

- For CMOS circuits is normally the same for all the capacitance C_i. One basic estimation is to expect that f_i is constant, for sample,

$$P = V^2 f \sum_i C_i = C_{total} V^2 f \longrightarrow (7)$$

Where C_{total} is the sum of all capacitance,f is the average frequency and V is the voltage swing.

Supply voltage of the circuit, switching of a node in the circuit is the main parameter that make sway on the energy, the peak power, and the average power utilization. Additionally, the clock frequency utilized amid testing that likewise make sway on the peak power, and the average power. The quantity of test patterns connected to the CUT, will make affect just on the aggregate energy utilization.

5. Low power testing plans:

There are general outline standards for making testable designs, for example,

- Avoiding logic redundancy
- Instatement of memory units
- Plan hardware to consistently global feedback loops.

These are 'adhoc' ways to deal with testable designs and in spite of the fact that they mitigate the testing issues, test vectors accomplishing high fault coverage are still extremely hard to make. The orderly way to deal with making a design more testable is alluded to outline for testability procedure. There are two general test strategies

- Scan path testing
- Built in self test

These strategies change the difficult issue of testing sequential circuitry into a simpler issue of testing combinational logic circuitry. They additionally give a more elevated amount systems testability approach, known as JTAG.

Numerous power diminishment techniques for testing have created. These methods are utilized to investigate either external testing or investigate the internal structure of configuration utilizing BIST or DFT.low power testing plan is partitioned into taking after classifications

- Low-power testing systems for external testing utilizing ATE, ATPG.
- Low-power testing techniques for internal testing utilizing BIST, DFT.

5.1 Low-power testing procedures for external testing:

5.1.1 ATPG algorithms for low power:

With regards to ATPG algorithm, it contains different procedures to diminish the power consumption amid external testing by ATE. This technique relies on upon the quantity of transitions in test data set. The late technique concentrates on ATPG algorithm which gives most extreme fault coverage as well as gives the greatest fault coverage at least conceivable power dissipation.

Heuristic strategy [4] to produce test sequences which make high power because of high and low frequency. A scan chain division algorithm [5] is utilized as a part of broadside testing application. It decreases shift and capture power. Low capture power ATPG and a power-aware test compaction strategy [6] brings down the development of test pattern count

contrasted with the detection number. Because of the detection number augmentations the peak power diminishes. The test compaction algorithm lessens test patterns count and average capture power.

5.1.2 Input data control methods:

In test mode, the switching activity must be diminished for lessening the test power. By distinguish an input control pattern, that pattern is applied to the essential inputs of the circuit amid the scan operation, so that the switching activity in the combinational part can be minimized or even dispensed with. The essential thought of input control method with existing vector or latch-ordering strategies [7] that decreases the power utilization.

5.1.3 Test vector ordering techniques:

The research has broadly investigated the test vector reordering strategies to diminish the switching power. Hamming distance based reordering [8] for compression of test data. Benefit of this methodology is a high standard compression with very low test power accomplished without including area overhead. Artifical intelligence based method [9] orders the test vectors in an ideal way to decrease switching activity during testing.

5.1.4 Taking into account don’t care filling:

ATPG produce uncompacted test data contains an expansive number of don’t care bits. The path-oriented decision-making (PODEM) algorithm allocate don't care bits available at the CUT inputs in a sharp way to reduce the quantity of transitions between two successive test patterns. Low capture power test generation for launch-off-capture Transition test [10] has utilized a genetic algorithm-based heuristic to allocate appropriate bits for don’t cares. This methodology creates a normal rate change in dynamic power and leakage power more than 0-fill,1-fill and minimum transition fill (MT-fill)algorithm for Don’t care filling. Segment-based X-filling [11] is utilized to diminish test power and retain the defect coverage. X-filling techniques minimize the aggregate weighted switching activity (WSA) amid scan capture operation. The patterns for don’t care filling is produced through automated test pattern generators, to form the patterns utilize minimum amount of power.

5.2 Low power testing procedures for internal testing:

5.2.1 Architecture of LFSR:

The Built-In Self-Test (BIST) architecture has two vital components: test pattern generator and response checker [12].To minimize the switching activity during test process adjusted Clock Scheme [31] is employed. Marginal hardware utilities

test pattern generator (TPG) for scan-based BIST [32] that might diminish switching activity in CUTS amid BIST furthermore accomplish intensified fault coverage with a sensible length of test succession. Both of these components use Linear Feedback Shift Register (LFSR).The LFSR can be intended to decrease the power utilization during test in the accompanying ways.

5.2.2 Diminishing the transitions:

These strategies lessen the transitions between consecutive patterns produced by LFSR and in addition between the successive bits in a given pattern. A dual speed LFSR plan [13] depends on two distinctive speed LFSRs to diminish the circuit's overall general internal activity by interfacing inputs that have hoisted transition densities to the moderate-speed LFSR. This procedure fundamentally lessens the average power and energy utilization without diminishing fault coverage. Cellular automated-based test pattern generators [14] successfully decrease power utilization while accomplishing high fault coverage. In weighted random pattern testing [15], the LFSR is altered by including weight sets to tune the pseudorandom vectors signal probabilities and as a result of that diminish energy utilization and expand the fault coverage. The LP-TPG [16] interpolate median patterns between the random patterns to diminish the transitional activities of primary inputs which in the long run lessens the switching activities inside the circuit under test, and hence, power utilization. New low-power BIST TPG plan [17] utilizes a transition monitoring window (TMW) that includes a TMW block and an MUX. This method subdues the transitions of patterns utilizing the k-value which is a standard that is gotten from the conveyance of TMW to examine over transitive patterns bringing about high-power dissipation in a scan chain. A low hardware overhead test pattern generator (TPG) for scan-based Built-In Self-Test(BIST) [18] that can diminish switching activity in circuits under tests(CUTs)during BIST. It likewise accomplishes high fault coverage with sensible lengths of test sequences. BIST TPG diminishes transitions that happen at scan inputs amid scan shift operations and subsequently lessens switching activity in the CUT. In LT-LFSR [19], transitions in LFSR are decreased in two measurements :(1) between successive patterns and (2) between serial bits. A low-power dynamic LFSR circuit accomplishes similar execution with less power utilization.

5.2.3 Creating valuable vectors only:

A lot of energy is squandered in the LFSR and in the CUT by futile patterns that do not confer to fault dropping. LFSR tuning changes the state transitions of the LFSR such that just the valuable vectors are created by fancied grouping

[20].To decrease such energy utilization, a mapping logic [21] is composed, which changes the state transitions of the LFSR such that just the valuable vectors are produced by coveted succession.

5.2.4 Separating nonessential vectors:

There are some nondetecting successions produced by LFSR. By repressing such vectors amid testing, over all switching can be lessened. A hefty portion of the pseudo-random vectors won't recognize fault notwithstanding devouring a lot of energy from the power supply [33] refinement approach is manipulated. A test-vector-inhibiting procedure [22] to shift through some nondetecting subsequences of a pseudorandom test set produced by LFSR. Decoding logic is utilized to reserve the first and last vectors of the nondetecting subsequences. A pattern-filtering strategy [23] is joined with Hertwig and Wunderlich's method to evade scan-path activity amid scan shifting. Hatami et al [29] suggested scan cell architecture that abatements power utilization and the aggregate consumed energy. This strategy taking into account the data compression, the test vector set is isolated into two rehashed and unrepeated segments. The rehashed part, which is basic among a portion of the vectors, is not changed amid the new scan path, where new test vectors will be occupied. Accordingly, the test vector is connected to the circuit under test in a less number of clock cycles, prompting a lower switching activity in the scan path amid test mode. [36] Handles the expanded activity amid test operation and it is used to manage hard-to-test circuits that encompass pseudo-random resistant faults.

5.2.5 Partitioning circuit:

Another methodology is circuit apportioning. Dividing the original circuit into sub circuits to accomplish the parallel testing. An effective scan dividing method lessens average and peak power in the scan chain amid shift and fuctional cycles. In low-power BIST technique [24] having the basics of circuit dividing, the procedure divides the original circuit into basic subcircuits so that two distinctive BIST sessions can progressively test each subcircuit.Low-power virtual test partitioning strategy [25],where faults in the glue logic between subcircuits can be recognized by patterns with low-power dissipation that are connected at the whole circuit levels, while the patterns with high-power dissipation can be connected inside of a divided subcircuit without loss of fault coverage. Approach for mapping every scan load to numerous PRPG seeds, figured with the goal that test pattern count, data aggregate and accordingly test cost are decreased [34].

6. Discrete testing technique for memory: Different transition decrease methods for memory testing is established by rearranging read and write access.A row bank-based precharge method based on the divided word line(DWL) architecture

is proposed in [30]. In low-power test mode, instead of precharging the whole memory array, only the current accessed row bank is precharged. This will result in significant power saving for the precharge hardware, with the continually expanding number of memories implanted in a system on chip (SoC), power dissipation because of memory test has turned into a genuine concern. Because of the simple execution and high fault coverage, the march-like algorithms have been utilized for the flash memory testing [35].

7. Low-power Design-for-Test approaches:

In this method, some additional equipment is added to outline for diminishing the power utilization amid test. Clock dividing and clock freezing [26] and utilization of J-scan rather than customary MUX scan [27] are the illustrations of such techniques. This methodology includes to alters the on-chip outline equipment to decrease the power utilization amid test and consequently might be called plan for Low-power test (DFLPT).

8. Low-power Testing methods for IP core-Based SoC:

For core-based SoC design, BIST effectively coming as a portion of IP core presents a standout amongst the most ideal testing strategies since it permits protection of a design's intellectual property [28]. Such BISTs are most suitable to test the IP core in standalone mode, yet when the IP core is incorporated with different blocks to frame a complete system, they may not be suitable. So including some low-power plans at the time of system incorporation is vital. The structure of IP cores are regularly concealed from the system integrator, so neither any alteration to its inside scan chain nor any DFT insertion is feasible for IP cores.Further,any testing apparatuses like Automatic Test Pattern Generator(ATPG) or fault simulation cannot be connected to it. Such cores are accompanying prepared to utilize test data. This test data is utilized to test the core when it is in confinement and in addition when it is as a part of system after being incorporated to system. It is generally accepted that the core is straightforwardly accessible, and it turns into the undertaking of the system integrator to guarantee that the logic encompassing the core permits the test boosts to be connected and the delivered responses to be transported for assessment.

Conclusion:

This survey paper on low-power testing procedures begins with the reason and impacts of high-power consumption amid test, encompassing power and energy model. We have surveyed propelled strategies accessible for power diminishment amid test and related issues to test power lessening for IP core-based SoC. In the close future, we can do change in power

lessening and afterward optimization with other critical test parameters like test application time, on-chip area overhead, test data compression.

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