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MAJORITY FUNCTION COMPUTATION USING DIFFERENT VOTER CIRCUITS - A COMPARATIVE STUDY

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Abstract

The scaling of CMOS circuits to the nanometer technology certainly increases the reliability concerns, extremely affecting the performance of circuits and poses a challenge to the future IC design. These reliability issues are due to different sources and it becomes sterner with continuous scaling. So, the reliability of a system is to be improved in CMOS VLSI circuits. The main basis for using a voter circuit is to apply redundancy in circuits for better improvement in reliability. The number of voter circuits have been studied and tested for layout power, area and delay and number of transistors required. This study implements two more new voting circuits using MUX and Carry Look Ahead Adder (CLA) techniques along with conventional existing majority functions. All the simulation results are obtained using a Microwind which is a layout editor with 90 nm process technology.

Keywords: Majority Function, Multiplexer, Reliability, TMR, Voter.

Introduction

In the two decades CMOS technology has maintained an inimitable position in modern digital circuits. CMOS processes have been scarcely improving for more than 20 years and will recommence to do so far at least the next decade. Designing reliable CMOS chips involves understanding and inscribing the potential failure modes. Reliability problems not only cause the integrated circuits to fail persistently but also cause the system to crash or misplace the data [1].

For designing reliable CMOS circuits, it is imperative to identify the fault in the circuit. Faults can occur due to various reasons in CMOS VLSI circuits. Most prominent among them is due to flaws and variation fabrication process. The

fault may be systematized as transient and permanent fault. Permanent faults are caused by miserable failure of the component whereas transient faults are inspired by temporary defect of the components or by the external disturbances such as noise, power dips and glitches [2]. To improve the reliability of the system, these faults should be vanquished by introducing complementary approach called Fault Tolerance. Even though there is a failure in some of the component, computation continues to provide the result is known as fault tolerance. However, in fault tolerance approach, faults may occur during functioning of a system. To overcome the effect of fault, Redundancy is added. Redundancy means adding information and resources, these resources includes hardware redundancy, information redundancy, software redundancy and time redundancy. Hardware redundancy depends on voting system to conceal the occurrence of faults. Now, the majority function takes place in the CMOS VLSI circuits. Triple Modular Redundancy (TMR) is the basic hardware redundancy in which two more similar modules are added along with the original module. The rest of this study is organized as follows: Section 2 contains the design of different voter circuits. Full adder with TMR using modified voter circuit implementation is explained in section 3. Section 4 provides the experimental result for voter circuits in terms of power, area, delay and transistors required. Finally, conclusion and works to be done in the near future are summarized in section 5.

2. Voter Circuit for Majority Function

Optimal designs of hardware voters with respect to gates, power dissipation and delay are studied in order to obtain high reliability in CMOS VLSI circuits. Voters are bit voters that compute the majority function on given input bits. Existing voter circuit with NAND and NOR gates and Modified voter circuits with MUX and CLA principles are discussed in this section. 2.1 Fundamental Voter Circuit: Here, the majority function is computed using carry out of a single-bit full adder as shown in Fig. 1. The expression for the fundamental voter circuit (voter1) [2], [3] is as follows,

$$V = AB + BC + AC \quad (1)$$

Where V is the majority output and A, B, C are function modules.

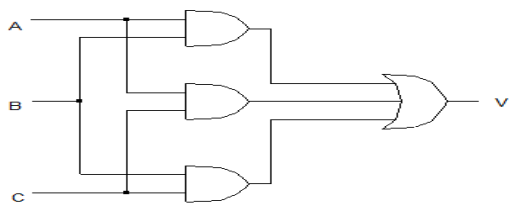

Fig-1: Majority function using AB + BC + AC (voter1).

2.2 Using Nand and Nor Gates: The NAND and NOR gates are so popular due to the easy implementation in the CMOS VLSI design field. Fig. 2 and Fig. 3 represents the majority function using NAND and NOR gates. Considering the voter circuit shown in Fig. 2, NAND operation will produce the majority value as the output [4]. For Example, if A = 1, B = 0, C = 1, then output V = 1 i.e., majority value will be the output.

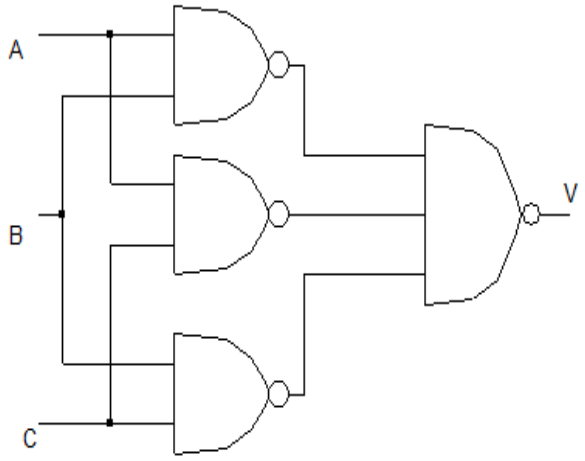

Fig-2: Majority function using NAND gates (voter2).

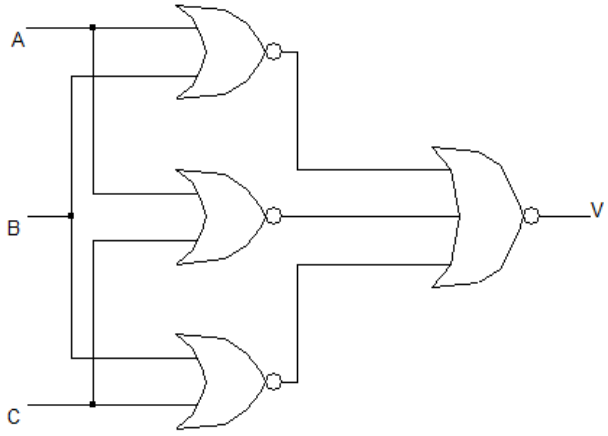

Fig-3: Majority function using NOR gates (voter3).

2.3 Voter Circuit Using Carry Look Ahead Adder Principle: CLA is a type of fast adder and executes voting function by means of carry look ahead addition. CLA computes the carry function based on complex gates. The main concept behind CLA is to improve the speed by reducing the amount of time required to deduce the carry bits. Fig. 4 and Fig. 5 represents the existing and modified voter circuit. In modified voter circuit, XOR gate is replaced with OR gate to acts as a voter. OR gate is chosen because it consumes low power and area and number of transistors requirement is less, which is verified in this study. The expression for modified CLA (voter5) is as follows,

$$V = (A + B)\,C + AB \qquad (2)$$

Where V is the majority output and A, B, C are the function modules.

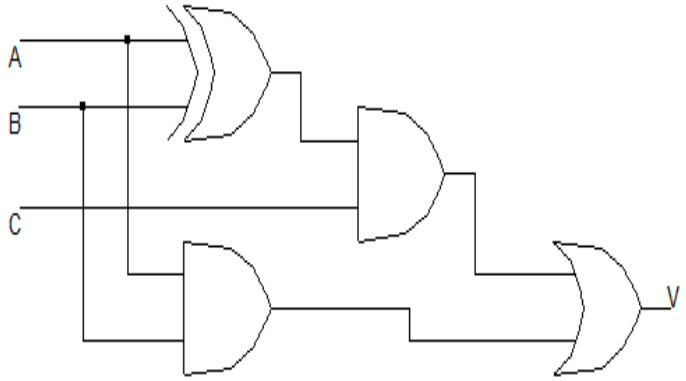

Fig-4: Majority function using CLA technique (voter4).

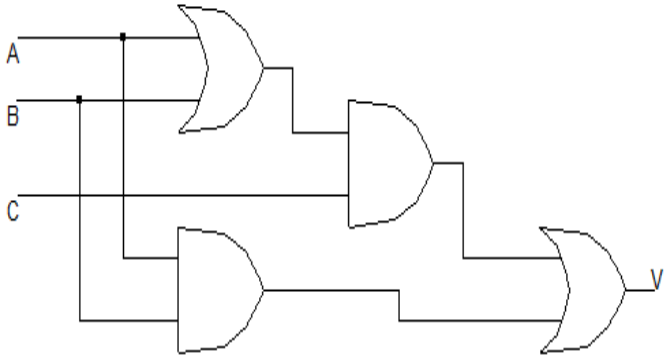

Fig-5: Majority function using (A + B) C + AB (voter5).

2.4 Using Mux and Xor: In the voter circuits shown in Fig. 6 output of XOR gate is always used as select line of the multiplexer in order to provide the majority value as the output [5].

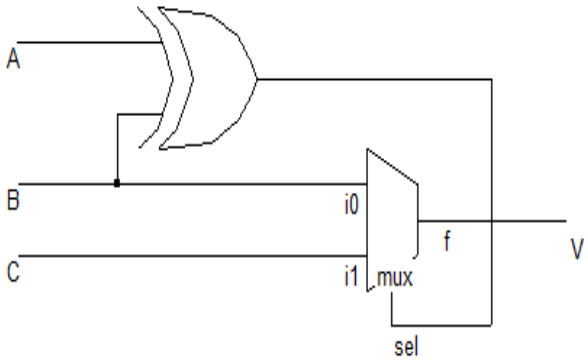

Fig-6: Majority function using MUX and XOR (voter6).

2.5 Using Mux: In the voter circuit shown in Fig. 7 multiplexer decides whether AND or OR operation should be performed based on select line. Modified voter circuit implies that multiplexers alone are sufficient to act as a voter i.e., provides majority value as the output which is shown in Fig. 8 and Fig. 9. Thus the modified voter circuit is optimized (power, area, delay and no: of transistor).

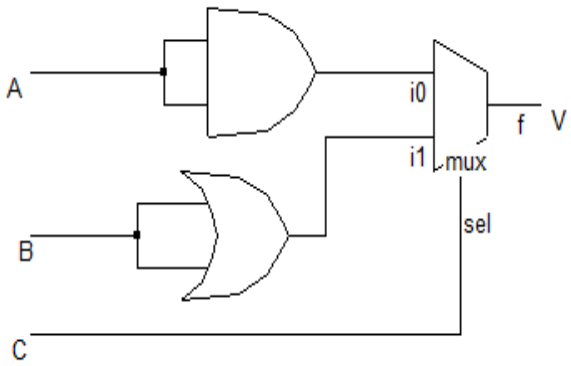

Fig-7: Majority function using MUX (voter7).

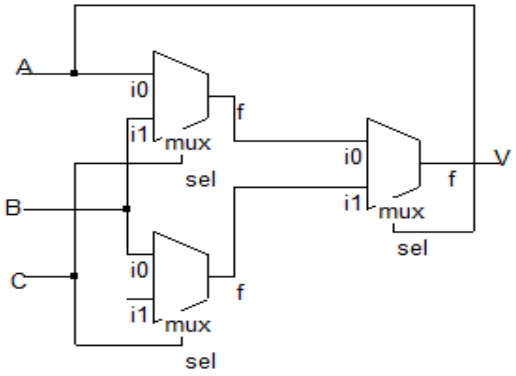

Fig.-8: Majority function using MUX (voter8).

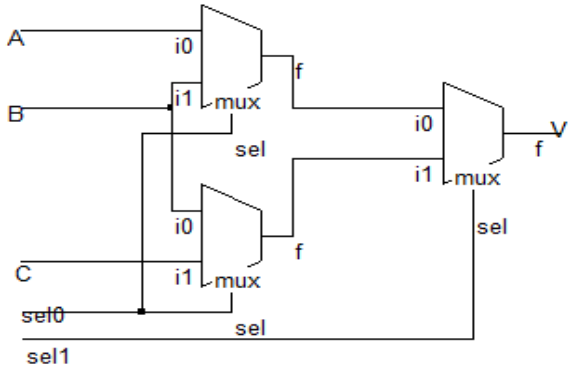

Fig-9: Majority function using MUX (voter9).

3. TMR Topology with Full Adder Using Modified Voter Circuit

A full adder can be implemented in many different ways such as with a custom transistor-level circuit or composed of other gates. The implementation of all voter circuit with and without full adder can be done. Full adder with TMR using voter circuit is described in this section. In Fig.10 Three Full adder are used with two modified voter circuit (voter7) to produce two outputs (sum and carry). Output of the first full adder is sum and carry, in which sum is given as first input to the first MUX based modified voter circuit and carry is given as first input to the second voter circuit. Likewise, all the sum are given as input to the first voter circuit and all the carry are given as input to the second voter circuit to produce two final output. Implementation of MUX based modified voter circuit for three full adder is shown in Fig. 10. Similarly, it is possible to implement three full adder with all other voter circuit discussed in this study. With slight modification full subtractor can also be implemented for modified voter circuit.

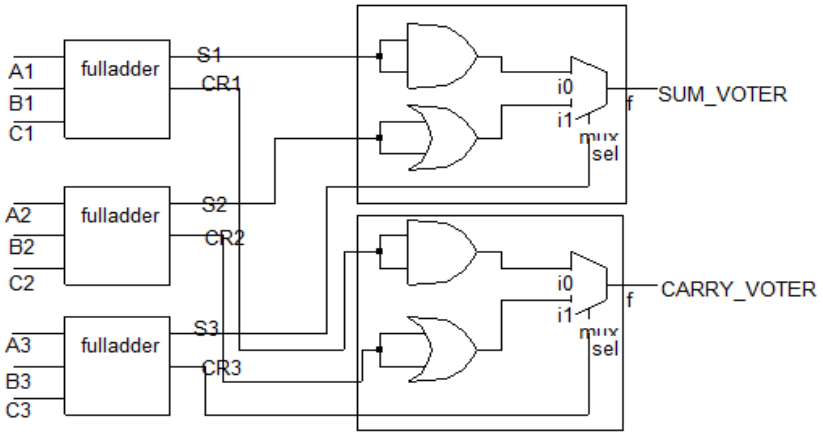

Fig-10: Full adder with TMR using MUX based modified voter circuit.

4. Results and Discussions

Comparison of all voter circuit with and without three full adder in terms of power, area and number of transistors required are discussed below for 90nm in Microwind tool. Fig. 11, 12, 13 and table1 represents the results of power, area, number of transistors and delay are tested for existing and modified voter circuits.

Table-1: Propagation delay results without full adder (90nm).

Voters	Rise delay (ps)	Fall delay (ps)
Voter 1	23	31
Voter 2	1016	19
Voter 3	14	18
Voter 4	23	24

Voter 5	7	40
Voter 6	25	58
Voter 7	23	19
Voter 8	22	21
Voter 9	22	_

Comparing all the modified voter circuits with three full adder performances, power dissipation is moderate in voter5 and voter7. Generally, NAND and NOR voter circuits consumes less power in CMOS VLSI circuits is illustrated in Fig. 14. Apart from NAND and NOR voter circuits, voter 5, 6, 7 requires reasonable area is shown in Fig. 15. Number of transistors needed is less in voter7, 8, 9, excluding NAND and NOR voter circuits is shown in Fig. 16. Delay with respect to output (sum) is reduced in MUX based voter circuit (voter 7) and delay with respect to output (carry) is reduced in modified CLA based voter circuit (voter5) shown in table-2.

Table-2: Propagation delay results with full adder (90nm).

VOTERS	SUM		CARRY	
	Rise delay (ps)	Fall delay (ps)	Rise delay (ps)	Fall delay (ps)
Voter 1	154	377	82	96
Voter 2	1139	372	71	92
Voter 3	1147	354	77	76
Voter 4	1153	-	97	85
Voter 5	1153	365	95	84
Voter 6	163	-	1061	1438
Voter 7	147	-	1080	1075
Voter 8	209	1856	1110	-
Voter 9	209	1856	1110	-

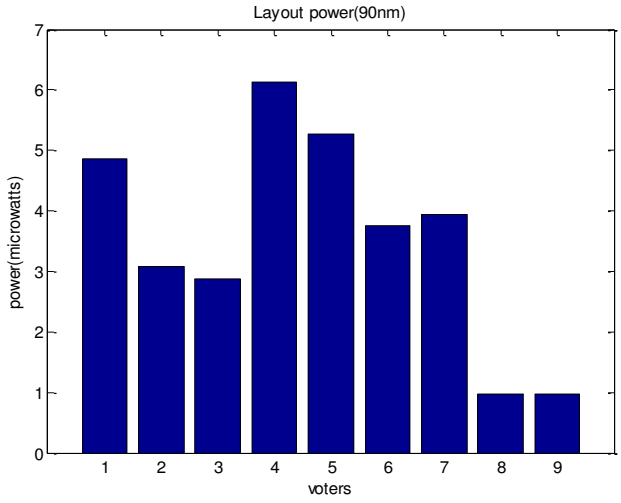

Fig-11: Power Dissipation for different voters (90nm).

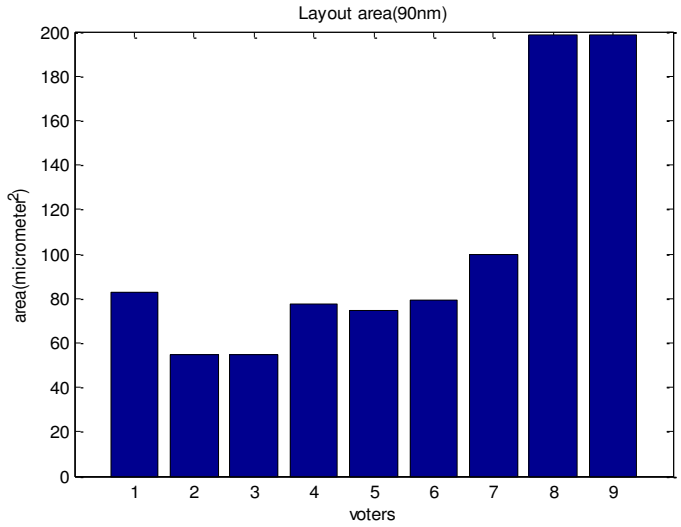

Fig-12: Layout area for different voters (90nm).

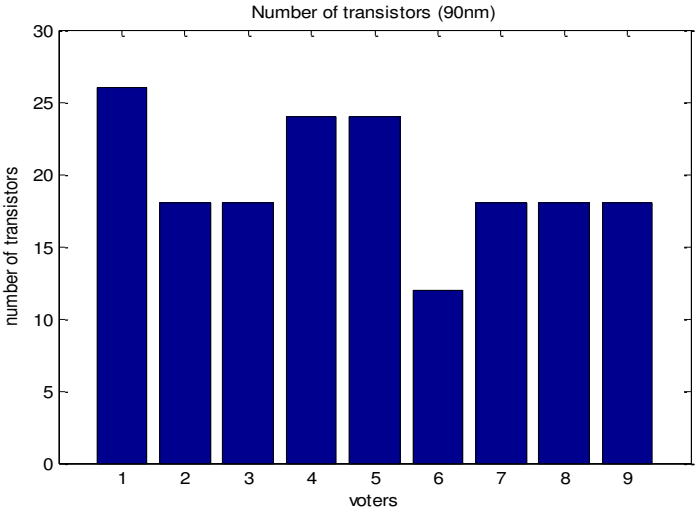

Fig-13: Number of transistors for different voters(90nm).

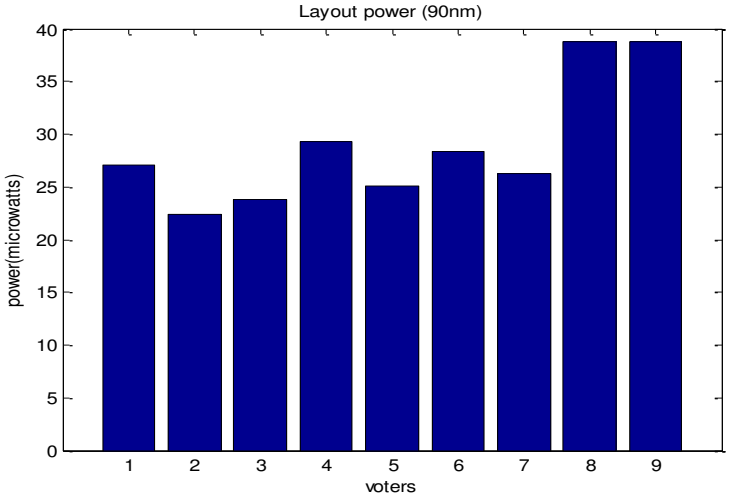

Fig-14: Power Dissipation of different voters with full adder (90nm).

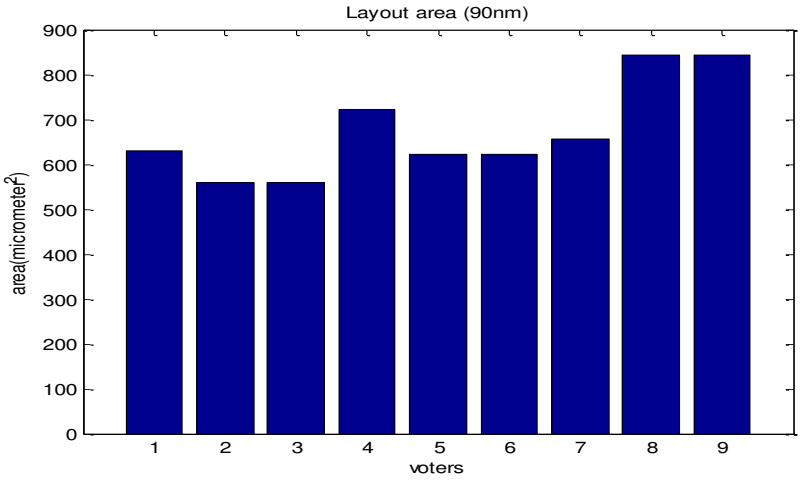

Fig-15: Layout area for different voters with full adder (90nm).

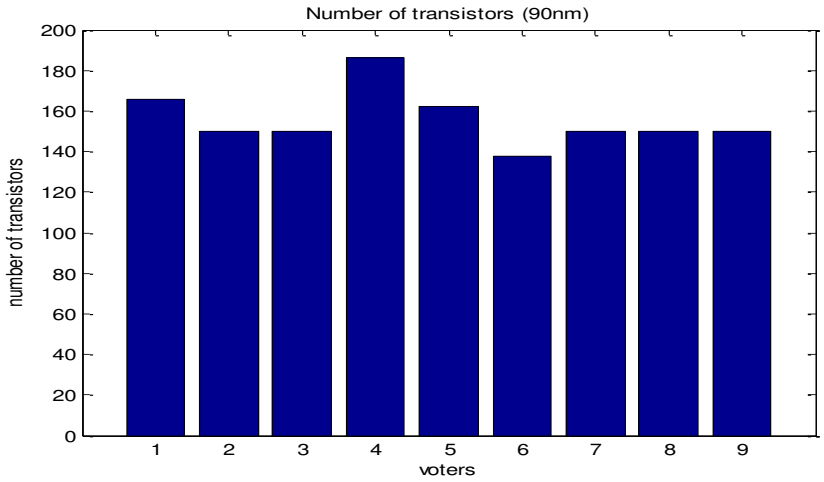

Fig-16: Number of transistors for different voters with full adder (90nm).

5. Conclusion

The design of different existing and modified voter circuit based on commercial 90nm CMOS technology is discussed in this study. These voter circuits are designed for improving reliability in CMOS VLSI circuits. The modified and existing voter circuits are analyzed and tested in terms of power, area, delay and number of transistors in Microwind tool. The future work can be extended in such a way that faults are introduced in this voter circuit and all the circuits in this study will acts as perfect voter even though fault is introduced and can be implemented in full adder and full subtractor with TMR technique.

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