ISSN: 0975-766X
CODEN: IJPTFI
Available Online through *Research Article*
www.ijptonline.com

AN EXTRAORDINARILY PERCEPTIVE ULTRA-LOW-POWER APPROACH FOR LOGIC DEVICES OPERATING IN SUBTHRESHOLD VOLTAGES

J.Surendiran[1], K.Subramanyam chari[2], T.Puvirajan[3]
Professor[1], Assistant Professor[2,3]
CMR Engineering College[1,2,3], Tamilnadu, Chennai.
Email: Surenjaya1981@gmail.com

Received on: 18-08-2017 *Accepted on: 28-09-2017*

Abstract

Biomedical devices that are implanted with human body require low energy delivery that results from various subsystems of the device. The stringent energy constraints dominate architectural and implementation decisions throughout the design of biomedical systems. This paper deals with balancing the trade off between power and performance at the two extreme ends of the design spectrum, namely the ultra-low power with acceptable performance in one end, and high performance with power within limit at the other.

Thus static CMOS logic circuits are analyzed in sub-threshold voltages to design the logic blocks with minimum energy consumption. Power consumption of the circuits with normal supply voltage is compared with the power of the circuits operating under ultra low voltages. In this paper static CMOS with different body biasing schemes that allows bulk CMOS circuits to operate efficiently at sub-threshold as well as above threshold voltages is introduced.

The simulations have been performed at the 180 nm technology node.

Keywords: Ultra-low power, Sub-threshold circuits, body biasing, Ring oscillator.

1. Introduction

Logic gates are the fundamental building block for high performance data path circuits and they continue to be a topic of interest especially as technologies are scaled to the nanometer regime. However increased leakage currents have led to the design of sub-threshold circuits that use these currents to drive the logic [1].A ring oscillator is a device composed of an odd number of NOT gates whose output oscillates between two voltage levels, representing true and false. The NOT gates, or inverters, are attached in a chain; the output of the last inverter is fed back into the first. A ring-oscillator based ADC (ring-ADC), which is entirely synthesizable, robust against switching noise, flexible resolution control employs this approach of ultra-low power circuits operating in sub-threshold voltage.

Some of the applications include devices such as digital wrist watches, radio frequency identification (RFID), sensor nodes, pacemakers and battery operated devices such as, cellular phones. Section 2 presents the motivation for power reduction in various applications. Section 3 presents configuration of the logic families that provides more current in sub-threshold. Section 4 presents the proposed work of MOS (transistor - pMOS/nMOS) devices in ultra-low power. Section 5 shows power estimation for different body biasing schemes with static CMOS. Section 6 shows the simulated results of the logic circuits at sub-threshold voltage. And section 7, is a comparison of body biasing schemes in different logic styles presented, offering designers a choice of improved speed, ultra-low power or a good speed-power trade-off.

2. Motivation of Power Reduction

In sub-threshold circuits, the supply voltage is reduced well below the threshold voltage of a transistor. Due to the quadratic reduction in power with respect to the supply voltage, sub-threshold circuits are classified as ultra low-power circuits.

Specifically in application areas where performance can be sacrificed for low-power, sub-threshold circuits are an ideal fit. Up until now, the power consumption has not been of great concern because of the availability of large packages and other cooling techniques having the capability of dissipating the generated heat. Another factor is the increased market demand for portable consumer electronics powered by batteries.

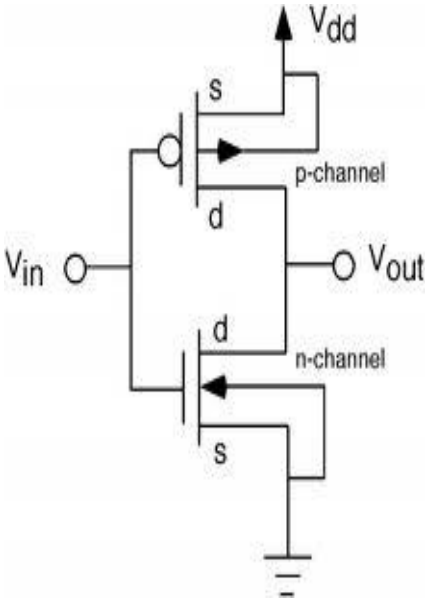
For these high performance portable digital systems, running on batteries such as laptops, cellular phones, personal digital assistants (PDAs) and biomedical instruments, low-power consumption is a prime concern. Hence, low-power ring oscillator (using logic gates) design has assumed great importance as an active and rapidly developing application in VLSI. Due to their extreme low power consumption, sub-threshold design approaches are appealing for a widening class of applications.

3. Logic Families in Sub threshold

Analysis of different logic styles operating in the sub-threshold region is essential. This could provide a designer with a meaningful choice depending on what the design calls for: speed, power, reliability (based on noise margins), or a good compromise between high speed and ultra-low power. The study provides some insights on different logic style performance in the sub-threshold region. In this paper static CMOS with standard body biasing is considered. Simple logic circuits that are a part of ring oscillator, such as inverter, 2 input NAND and 2 input NOR gates are analyzed under different body biasing schemes.

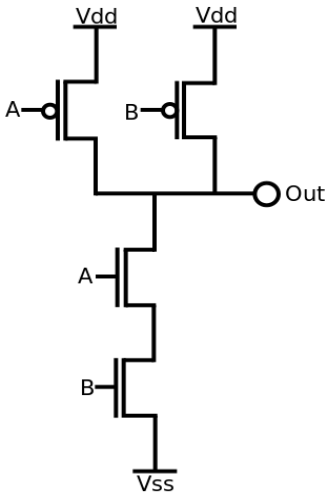
4. Proposed Work

In this paper logic circuits are operated with power supply Vdd less than transistors threshold voltage, Vt. This is done to ensure that all the transistors are indeed operating in the sub-threshold region. The voltage transfer characteristics of the inverter gate running in sub-threshold mode are closer to ideal compared to one in strong inversion region. The improvement is mainly caused by the increase in the circuit gain.

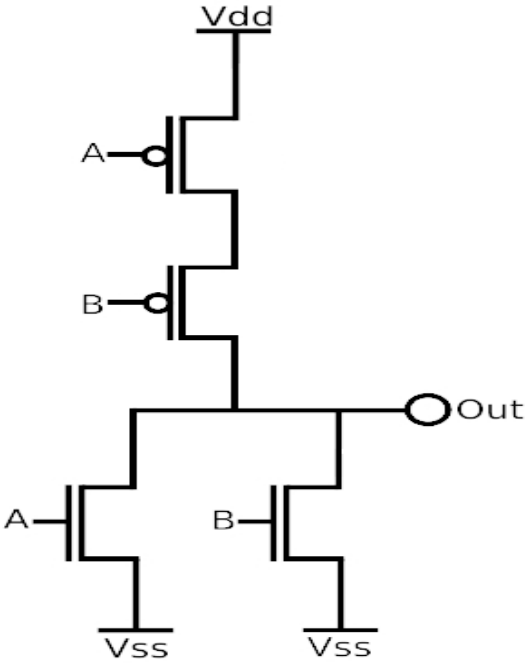


(a) CMOS Inverter

The merits of regular CMOS logic such as excellent robustness, good noise margin and low power consumption are inherited in sub- threshold region. Simulations have been performed at the 180 nm technology node. Table 1 shows the simulation results for Inverter, 2 input NOR, 2 input NAND gates in normal mode and sub-threshold regions. Comparison between the powers of the mentioned digital logic gates in both the regions was made. The figure 1 below shows the basic logic gates operating under sub-threshold voltage.



(b) CMOS NAND



(c) CMOS NOR

Figure 1: Static CMOS logic circuits.

5. Power Estimation for Different Body Biasing Schemes with Static CMOS.

A technology is often characterized by estimating the speed of the design that would be fabricated using this technology. This is done by a ring oscillator circuit, which is a chain of odd numbers (typically 3 or 5) of minimum size inverters. The ring oscillator is utilized to characterize the maximum operating speed of new fabrication process technology. The last inverter's output is connected to the input of the first inverter as shown below.

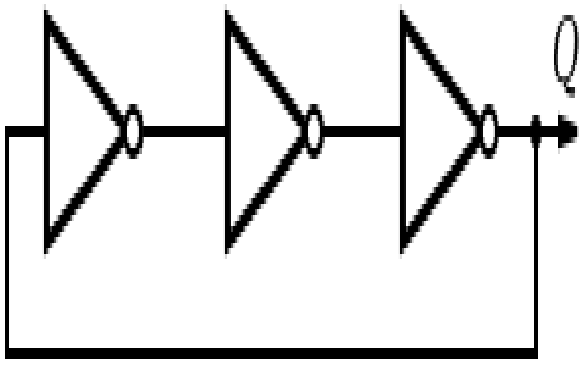
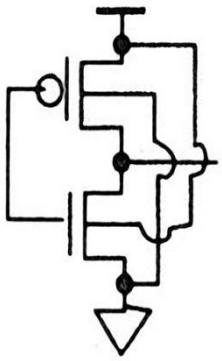
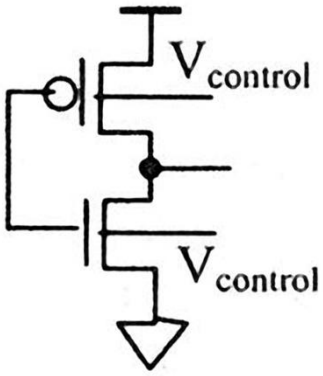


Figure 2: Three-stage ring oscillator circuit

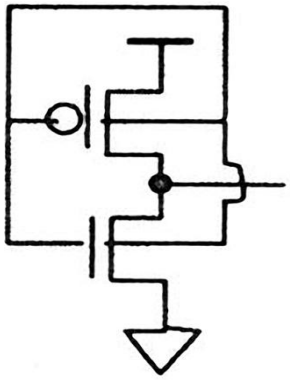
The performance evaluations of static CMOS under different body biasing scheme configurations was done and is shown below in figure 3. The results show that swapped body biasing, dynamic threshold CMOS and the tunable body biasing schemes all lead low power consumption. Figure 3 shows the transistor configurations for each of the body biasing schemes that have been simulated in 180 nm regime. In sub-threshold voltages DTMOS, SBB and TBB outperform the traditional body biasing technique.



(a) Swapped Body Biasing



(b) Tunable Body Biasing



(c) DTMOS

Figure 3: Different Body Biasing Schemes.

The powers obtained as a result of body biasing schemes are shown in the following table 1.

BODY BIASING SCHEME	POWER
Swapped	0.295 µw
Tunable	0.297 µw
DTMOS	0.286 µw

(a) Body Biasing Scheme - Inverter

BODY BIASING SCHEME	POWER
Swapped	0.276 µw
Tunable	0.279 µw
DTMOS	0.257 µw

(b) Body Biasing Scheme - NAND

BODY BIASING SCHEME	POWER
Swapped	0.282 µw
Tunable	0.281 µw
DTMOS	0.286 µw

(c) Body Biasing Scheme – NOR

Table 1: Comparison of power.

7. Comparison of Body Biasing Schemes in Different Logic Styles

Comparison of power at different traditional mode supply voltages and sub-threshold voltages are shown in table 2.In the strong inversion region, the static power consumption was due to transistor on – current, which is orders of magnitude larger than off current. In the sub-threshold region, however the short circuit current is also weak inversion current which is relatively much less significant.

V	INVERTER	NAND	NOR
1V	1.343 µw	1.563 µw	1.236 µw
0.3V	0.296 µw	0.276 µw	0.292 µw

Table 2: Comparison of power at sub-threshold and normal supply voltages

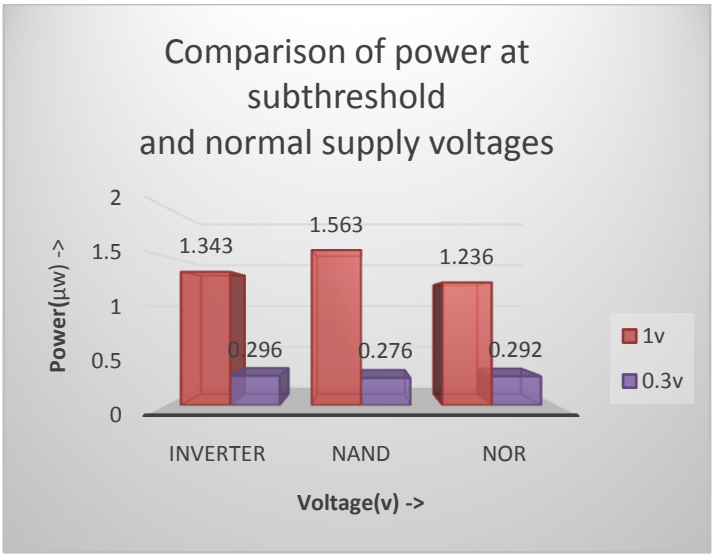


Figure 4: Comparison of power at sub-threshold and strong inversion region.

8. Conclusion

This paper focuses on various digital circuits operating in sub threshold region for achieving ultra low power. The relevance of different logic styles operating in the sub-threshold regions considered concluding that the power obtained at the sub-threshold voltage of CMOS inverter, NAND and NOR gates is considerably less when compared to that of supply voltage.

The paper has also obtained power at different body biasing schemes namely swapped, tunable and DTMOS. However, due to its slow performance, sub threshold circuit is limited to only certain applications, where ultra-low power is the main requirement, and performance is of secondary importance.

References

1. Soeleman, H., Roy, K. and Paul, B. C. "Robust Subthreshold Logic for Ultra-Low Power Operation," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 9, No 1, February 2001, pp. 90-99.
2. Kao, J., Narenda, S. and Chandrakasan, A., "Subthreshold Leakage Modeling and Reduction Techniques," IEEE/ACM International Conference on Computer Aided Design (ICCAD), November 10-14, 2002, pp.141-148.
3. S. Yang, W. Wolf, N. Vijaykrishnan, T. Xie and W. Wang, "Accurate Stacking Effect Macro-Modeling of Leakage Power in Sub-100 nm Circuits," 18"' International Conference on VLSI Design, 2005, pp. 165-170.
4. A. P. Chandrakasan, S. Sheng and R. W. Brodersen, “Low Power CMOS Digital Design,” IEEE Journal of Solid-stateCircuits, vol. 27, no. 4, pp. 473-484, April 1999.
5. C. Hyung-II Kim, H. Soeleman and K. Roy, "Ultra-Low- Power DLMS Adaptive Filter for Hearing Aid Applications," IEEETransactions on Very Large Scale Integration (VILSI) Systems, Vol. I1, No. 6, December 2003, pp. 1058-1067.
6. Logic Circuits Operating in Sub threshold Voltages Jabulani Nyathi and Brent Bero School of EECS Washington State University
7. Ultra-low power digital logic circuits in sub-threshold for biomedical applications K. Ragini, Dr. B.K. Madhavi
8. Frenkil.J “A Multilevel Approach to Low- Power IC design,” in IEEE spectrum Vol.35, PP.54 -60, February 1998.
9. Chandrakasan, A.P, “Low-Power CMOS Digital Design” in IEEE Jl of Solid state circuits.
10. M. Horowitz., et. A1, “Low Power Digital Design”, IEEE symposium on Low Power Electronics 1994, pp. 8-11.