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SYNTHESIS OF SINGLE SERIES GENERATORS WITH REARRANGEABLE PULSE DURATION AND ITS NUMBER IN SERIES

Elena Nikolaevna Korobkova, Vasily Grigorievich Rubanov, Alexander Geraldovich Bazhanov
Belgorod State Technological University n.a. V.G. Shukhov
Russia, 308012, Belgorod, Kostukova st., 46.
Belgorod State Technological University n.a. V.G. Shukhov
Russia, 308012, Belgorod, Kostukova st., 46.
Belgorod State Technological University n.a. V.G. Shukhov
Russia, 308012, Belgorod, Kostukova st., 46.

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Abstract.

It is proposed the synthesis method of a series pulse generators with rearrangeable parameters, based on the representation of the designed automaton as a functional-block composition of several interconnected separate units, each of which defines one of the formed timing pulse sequence. Such generators could form the impulses sequence for low level parts of control device to quick forming the reference values. From this point of view it could be used in control structure for more accurate positioning of robot operating element or as reference value in complex control system. This article contains the recommended internal structure of pulse sequence generators and their tuning algorithm in linking with the following devices, which could be placed after it in control system.

Keywords: digital automata, decomposition, logic functions, synthesis, minimization, control system, pulse sequence generator, Karnaugh maps.

Introduction.

In connection with the rapid development of programmable integrated circuits and their implementation in practice of digital devices designing [1] there is again increased the interest in logical synthesis not only at the level of computer-aided design, but also at a lower – "manual synthesis" level.

This article is devoted to the synthesis of pulses series generators with adjustable (programmable) parameters used in the construction of various generators of discrete time intervals, encoding and decoding devices, programmable interval timers, stepper motor control devices, control devices for firmware automata with rearrangeable duration of microinstructions, sequence diagram generators and so on.

Analysis of researches and publications devoted to the problem of designing units and nodes, many of which are

included in the library of standard elements, is the subject of many works, a simple listing of which is by no means a trivial task [2].

It should be noted that in spite of sufficient range of known libraries of standard components, which are the main bricks in the arsenal of digital devices developers, the generators of pulses series with rearrangeable parameters are not represented.

The known methods of design allow constructing any finite automaton by a given algorithm. Constructing the finite automaton with a rigid logic does not cause any problems for the case of the fixed parameters of the output signals. When designing an automaton with rearrangeable parameters, there are problems not even connected with the schemes synthesis of the automaton itself, but with finding the optimal variant of the scheme with the minimum number of inter-element links and minimum complexity of the functions representation that define the automaton settings to the specified parameters.

The method of digital automata synthesis, based on the concept of logic functions in a generalized form, which simplify the automata synthesis procedure with rearrangeable time parameters, is offered in [3, 4].

The article objective is to continue research aimed at developing nonconventional methods of digital automata synthesis with rearrangeable parameters and their application to the digital automata synthesis such as pulse series generators.

The solution method. The proposed in [5] method is based on the representation of projected automata as a functional-block composition with several interconnected separate units, each of which, regardless to the number of bits, allows us to treat the composition units as the simplest memory elements having two states: the low state (if the value of all bits in the unit is equal to zero) and high state (if at least one bit in the unit is equal to one), and projected automaton as a whole as a device consisting of two (or more) such elements. The number of units equal to the number of time parameters of formed output sequence. Each unit is a finite cyclic digital automaton.

We can use the following units as standard blocks: any binary, binary code decimal summing, subtracting or reversible counters, count-conversion circuits with any conversion factor and with any states encoding; cyclic automata, made by shift registers (counters with a unitary coding, Johnson's counters and linear meters).

When exposed the clock pulse one or more units can remain in the same state (storage mode), can transfer to the next state in accordance with the algorithm of this unit operation (serial transfer mode), can change the direction of sequential transition (reversal), can go to any state of its sets, defined by external control word (parallel loading

mode), can go to the initial (zero) state (zero setting mode). To allow these transitions each unit must have the corresponding inputs, on one of which the formation of the active signal (equal to 0 or 1 depending on the selected scheme) provides the selected mode.

Main part. Design a predetermined finite automaton starts with its verbal description, followed by drawing the transition table as in the case of classical methods. In classical methods of design the total number of variables is the sum of all the bits of the automaton as a whole and the number of tuning variables, so the number of table sets (including unused) is 2^{k+v}, where k – the number of memory elements (latches, bits) of the designed automaton as a whole, v – number of tuning variables. In the proposed method the total number of sets of tables (equal to 2^n, where n – the number of units) depends only on the number of used units bits and the number of tuning variables regardless to the number of used blocks bits and the number of tuning variables. That significantly reduces the total number of sets of the transition table in comparison with its classic view.

The automaton transitions chart represents in the form of closed rings equal to the number of units included in the composition with a common vertex, corresponding to the initial (zero) state of each block.

In such representation each subsequent state S^{r+1} of a separate unit in (r+1)-th cycle depends not on its particular state S^r in the present cycle, but on the state of all units. Unit state characterized by a signal value F_i on it output (in particular on the output of the transfer in the case of the subtract counter), and the general automaton state in (r+1)-th clock cycle is determined by values of the signals at the outputs of all units in the r-th cycle.

After selecting the appropriate number and type of units determined in accordance with the descriptive algorithm (given orthographic drawings and charts) we should compose a table of transitions and combined with it tables of modes and excitation functions (values of the control signals that provide a transition from the current state to the following) in accordance with the above chart. Transition table contains 2n columns (n – number of blocks). The first n columns list all combinations of signal values (variables) on the unit output (even if some combinations not used in the automaton functioning) in r-th cycle and n columns that shows the signal values (variables) at the unit outputs in the (r+1)-th clock cycle.

Modes table of settings contains n columns in each line of which is commented the setting mode of unit on this combination of signal values in the r-th clock cycle. In accordance with modes table of setting the excitation (control) functions table is filled. It contains the number of columns equal to the number of required control signals generated at the inputs of a sets L, $D_0 – D_{n-1}$, P, R, U: L – enable input of parallel loading; ($D_0 – D_{n-1}$) – inputs of feeding the

loaded data; *P* – enable input of counting mode (serial transfer); *R* – input of setting to the initial state; *U* – input of control the transfer direction (reverse). The number of involved (required) control inputs in each unit depends on the algorithm of functioning the automaton as a whole and the way of partition it into units.

The table is filled in accordance with the above commentary of units reaction (setting modes) for each of the combinations, it should be borne in mind that each of the control input is assigned a priority, so if a certain row of the table for some unit stamped the active value of the control signal (excitation function value) at the input, and it has a higher priority, then for the signals at the other inputs of the unit, which have the lower priority, can be fixed in 0 or 1 (redundancy sign). So the obtained table allows finding the necessary excitation (control) functions, defining the signals transmitted to the control inputs of each block. When finding the excitation functions the unused and redundant combination extends by definition of value 0 or 1, based on the requirements of the automaton structure to minimize or eliminate the risk. As the number of units, which is equal to the number of parameters of the output pulse sequence, does not exceed five, then the excitation functions and its circuit implementation are quite simple regardless of the total number of automaton bits and the number of setting variables.

The output signal more often is taken from the output of one of the units or is a function of output signals from several units. The output value is zero if all values of unit bits are zero. If at least one unit bit is equal to 1, then output value is equal to 1.

The designed device is intended for the formation of single series with rearrangeable pulse duration and its number in series. The pulse duration (equal to *BT*, *T* – period of clock cycle pulses) is determined by the binary word $B = b_{n-1}b_{n-2}...b_1,b_0$, applied to the settings input, the number of pulses in the series is determined by the binary word $N = n_{n-1}n_{n-2}...n_1,n_0$, applied to the second group of settings inputs. The pause between pulses is also fixed and equal to *T*.

The designed device will operate properly in the case if its construction ensures that when power supply is switched on all units will transit in the initial (zero) state. This requires each unit to provide the presence of setting input, on which the analog circuitry generates an active value of signal *R*. In addition, it is necessary to provide the presence of the start input (Start), the supply of the active signal value of which prepares all the automaton units to transfer into the states, determining the timing parameters of generated pulses.

Timing charts (orthographic diagrams) for representation the functioning algorithm of the projected generator for setting option, $B = 3$, $N = 4$ are shown in Fig. 1.

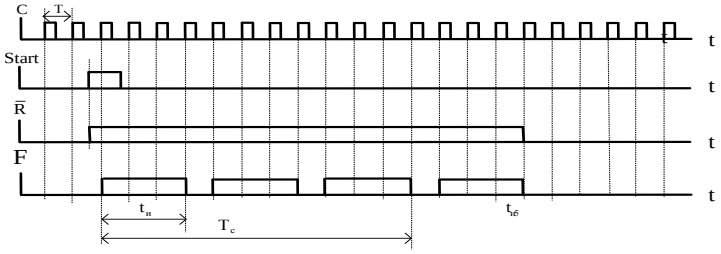

Fig. 1. The timing diagrams for representation the algorithm operation.

By analyzing the given diagrams we can conclude that the projected automaton is characterized by two adjustable parameters: duration and number of pulses. Therefore, the functions that define these parameters can be assigned to three units: a unit defining a series of pulse width, unit that determines the number of pulses in the series and the unit defining the setting of initial state, startup and return to the initial state after the formation of a given series.

The best option of the first and second units are typical reversible binary counters with enable input of synchronous parallel load *L,* inputs of supply the downloadable data $D_0 - D_{n-1}$, counting enable input and input of asynchronous zero setting. The number of counter bits determines the range of adjustment the duration and number of pulses in the series. After selecting the units number and type for detailed perception of automaton functioning algorithm and compilation the transfer table it is recommended to provide more detail generalized timing diagrams (Fig. 2) illustrating the operation of the algorithm with bringing the values of the signals at the counters outputs, aligning it with the contents.

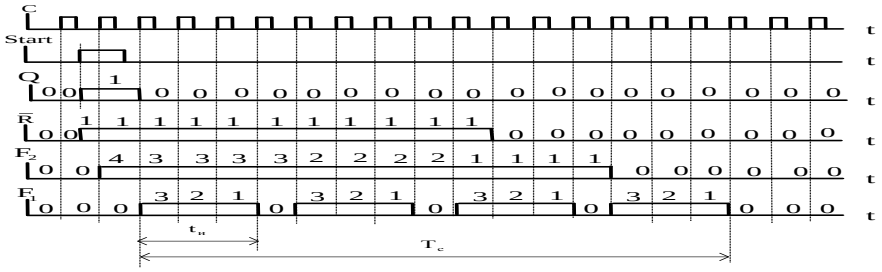

Fig. 2. Generalized timing diagrams.

The generalized transition chart (Fig. 3) consists of two rings with a common vertex, corresponding to the initial (zero) units state that define the adjustable parameters: lower ring – transition chart of the first counter; top ring – transition chart of the second counter. We believe that after the power supply is switched on for a period of time, determined by the speed of the element base, the units are set to the initial (zero) state. The signals at the outputs of the counters $F_2 = F_1 = 0$. The value of these signals (the null set of variables $F_2F_1 = 000$) provides a setting of the first and second counters on synchronous parallel load mode, and the latch – on the mode of transition to the state 1. This state should remain unchanged as long as not received the starting pulse. This function is assigned to the third unit

(start-stop device) that generates an active signal $\overline{R} = 0$ on the inputs of asynchronous zero setting of counters, blocking the zero state.

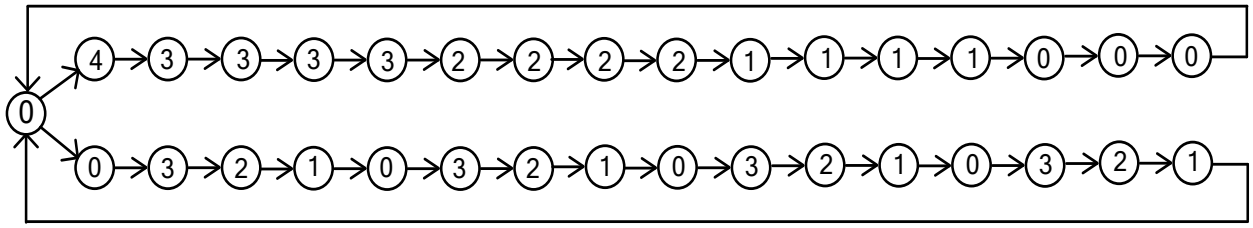

Fig. 3. Generalized generator transitions chart.

Receipt the start pulse on the input of start-stop device releases the lock (generates a signal $\overline{R} = 1$) and then at the time of arrival of the first (after unlocking) clock cycle pulse *C* the second counter goes into a state, defined by value $N = n_{n-1}n_{n-2}...n_1,n_0$, the zero state of the first counter remains unchanged. As a result, here is a setting of the second counter at the storage mode, and the first – at load mode. Then with the arrival of the next clock cycle pulse the first counter enters the state determined by the value $B = b_{n-1}b_{n-2}...b_1,b_0$ and the second counter state will remain unchanged. As a result of this transition the first counter is set to counting mode (subtraction) and the storage state of the second counter remains unchanged. Similarly with the arrival of the following clock cycle pulses the modes and appropriate transitions for all vertexes of the chart are determined. It should be noted that by the end of the formation of a series the start-stop device must be ready for generation the active signal on the input of asynchronous setting of zero state for all units.

The results of these considerations present in the form of a transitions table (the first four columns), combined with it modes table (the following two columns) and the table of the excitation functions (the last four columns). When representing the modes table and corresponding values of excitation (control) functions for indifferent combinations of sets are noted by the sign #.

Table 1: Modes table.

F_2	F_1	F_2	F_1	CT2	CT2	$\overline{L}_2$	$\overline{P}_2$	$\overline{L}_1$	$\overline{P}_1$
0	0	0	1	Load	Storage	0	#	1	1
0	0	1	0	Storage	–	1	1	1	0
0	1	0	0	–	Load	1	0	0	#
0	1	1	0	Storage	–	1	1	1	0

When filling the modes table used the following abbreviations: "Load" – load mode; "Storage" – storage mode; "–" –

subtraction mode; "#" – the value is indifference. To find the lowest form of the excitation (control modes) functions we should represent them in the Karnaugh maps with neighboring coding. Maps of allowing functions for loading the second counter ($\overline{L}_2$) and counting ($\overline{P}_2$) are shown in Fig. 4a and 4b respectively.

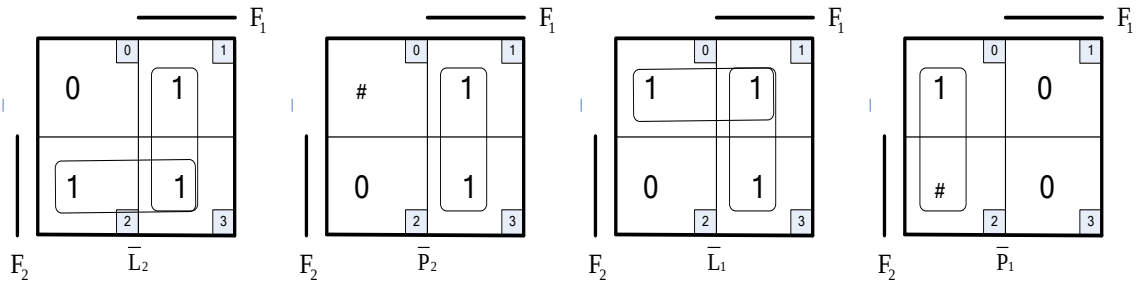

Fig. 4. Maps of allowing functions values.

Selecting the Boolean rectangles we record the minimum DNF loading allowing function $\overline{L}_2 = F_2 \vee F_1$ and counting allowing function for the second counter $\overline{P}_2 = F_1$.

Maps of loading allowing functions of the first counter ($\overline{L}_1$) and counting ($\overline{P}_1$) are shown in Fig. 4c and 4d respectively.

Selecting the Boolean rectangles we record the minimum DNF loading allowing function $\overline{L}_1 = F_2 \vee F_1$ and counting allowing function for the second counter $\overline{P}_1 = F_1$.

The circuit is built in accordance with the received expressions requires a circuit of detection the switching power supply that provides a transition to the initial (zero) state, the presence of the start input and ensuring the return to the initial state after the generation of a determined series. All these functions are performed by start-stop device which is built on a synchronous D-latch [6].

The generator circuit, which is constructed in accordance with given in [6] description of start-stop device and obtained above representations of control functions $\overline{L}_1$, $\overline{P}_1$, $\overline{L}_2$, $\overline{P}_2$, *U*, is shown in Fig. 5.

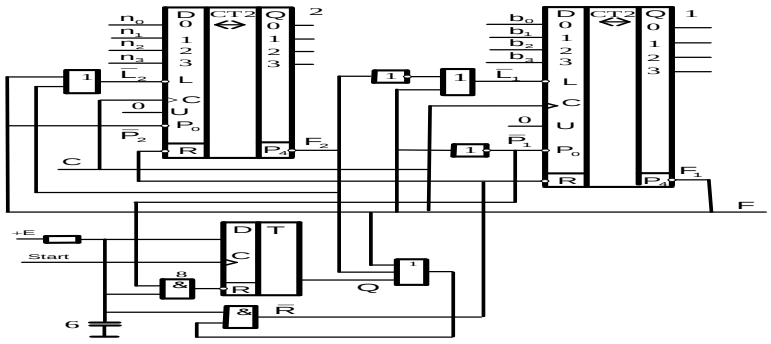

Fig. 5. Generator circuit.

The generator comprises three blocks, the first and the second of which are made on the standard counters and the third – on the synchronous D-latch, and a group of elements providing units control in accordance with a given operation algorithm. The represented functions of designed generator could be used as a part of hardware regulators in application described in [7 – 9] or in automatic robotic manipulator movement for it accurate positioning as reference former [10].

Conclusion. It is made the synthesis of a single pulse series generator with rearrangeable parameters, based on the representation of the designed automaton in the form of a functional-block composition of three interconnected separate units, the initial state of which is interpreted as a logic 0. Any other state of each of the composition units is treated as logic 1, ensuring thereby the independence of the number of sets number of bits of used units.

Outputs. The proposed method enables, in contrast to the known approaches, to reduce the total number of sets of state tables which greatly simplify the synthesis procedure as compared to known classical methods and to make more effective and quick low level schemes for control systems.

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