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FAULT-TOLERANT SYSTEM DESIGN USING 7-MODULAR REDUNDANCY CONFIGURATIONS

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Abstract

Objectives: In the current microelectronics trend, reliability is a major concern due to very large scale integration of transistors in a circuit. The hardware redundancy techniques are more popular to improve the reliability and hence the fault-tolerant systems are designed**.**

Methods/Statistical analysis: This study focuses main on the redundancy which is the key to design fault-tolerant systems. The fault-tolerance is achieved here by means of masking faults with voter circuits. The majority among the inputs is determined using voter circuit. In 7MR configuration, the voter circuit determines the majority among the seven inputs; this can tolerate only three errors in a system.

Findings: Three 7MR configurations are proposed based on 7MR using 5MR, 7MR using 3MR with additional logic, and 7MR using full adder; the results are compared with the existing 7MR architecture with industry standard benchmark circuits. The functional verification is done using DSCH and Micro wind electronic computer aided design (ECAD) software tools with power, delay, and layout area simulation results. The proposed architectures are tested with few industry standard benchmark circuits on Alter a FPGA device (EP4CE115F29C7) using Quartus II 13.1 synthesis software tool. The comparative results are obtained by a performance metric called figure-of-merit (FOM) using resource utilization, power, and critical path delay.

Application/Improvements: 7MR tolerant systems can be particularly useful in applications like aerospace, where the system can be malfunctioned due to the high energy cosmic particles strike.

Keywords: Fault-tolerant; FPGA; Hardware Redundancy; 7 Modular Redundancy, Quartus 13.1, VHDL.

I. Introduction: The reliability becomes very important in the mission-critical applications like banking systems, aerospace, defense communications, etc. These applications should run in real time without fail and hence fault-

tolerant systems are dominating in the field of microelectronics reliability. The hardware redundancy is often used to improve the reliability at the cost of area overhead. In the triple modular redundancy (TMR) configuration, two more duplicate copies of the original module are placed[1,2]. This produces fault-free response even though one system fails during the real time due to soft errors and hence can tolerate one error at a time[3,4]. In general, NMR configuration can tolerate (N-1)/2 errors if N is odd. For example, the 5MR configuration can tolerate two errors; the 7MR configuration can tolerate 3 errors and so on. In applications like aerospace, the system can be malfunctioned due to the high energy cosmic particles strike; this fault can be a temporary one or a permanent one[5]. The faults which are occurred only for a small period of time are referred to as temporary faults; these are known as single event transient errors[6].

The faults in a system can also be detected and corrected by the technique so called information redundancy. The redundant bits are added along with the original information for the purpose of error detection and correction[7]. The time redundancy would be another method to mitigate errors in system by means of doing the computations again if any errors are found.

This study focuses main on the redundancy which is the key to design fault-tolerant systems. The fault-tolerance is achieved here by means of masking faults with voter circuits[8]. The majority among the inputs is determined using voter circuit. In 7MR configuration, the voter circuit determines the majority among the seven inputs; this can tolerate only three errors in a system. The voter circuit can be designed easily using the carry out of a full adder circuit which acts as a majority function. This can be accomplished by "AB+BC+CA" where A, B, and C are the three function module outputs as in Figure 1.

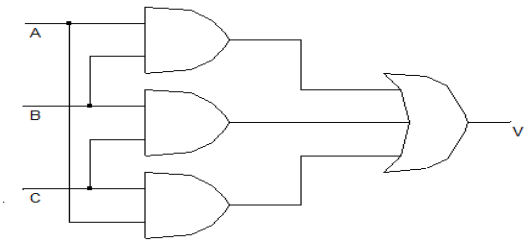

Figure1. The conventional voter.

The voter circuit can also designed using NAND and NOR gates. This can also be determined also using (A B) C + AB using the carry-look ahead adder concept. The majority function can also be found by using multiplexer, AND, and OR gates; if the A = 0, the voter output becomes as AB and if A = 1, the voter output becomes as A+B [9]. This study is organized as follows. The Section 2 contains the existing 7MR architecture and the Section 3 produce three

modified 7MR architectures. The Section 4 contains simulation results and discussion and the conclusions are mentioned in the Section 5.

II. Existing 7mr System

This architecture gives us a clear picture of seven modular redundancy circuit and this serves as the base architecture for further development of other architectures. The general motivation behind the development of 7MR is the requirement for the improvement of reliability of a system despite the fact that achieving it at the cost of area, power and critical delay. Thus to achieve better reliability 7MR was designed with the basic structure which was inclusive of basic logic units and Multiplexers[9, 10]. It is used to achieve a basic majority voter circuit which is designed to drive the majority function as the output. In this case the minimum majority is 4 out of 7 inputs. The Existing 7MR architecture is shown in Figure 2.

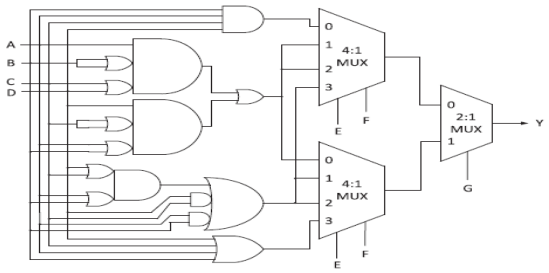

Figure-2. Existing 7MR Architecture

III. Modified 7mr Architectures

This section describes three proposed 7MR architectures using 5MR with additional logic, 3MR with additional logic, and using full adder.

A. 7MR using 5MR with additional logic(Architecture I)

This architecture consists of 2 stage system. The first stage consists of standard 5MR, combinational circuit, and decoder circuits. The second stage involves use of a 4x1 multiplexer. The main requirement of the multiplexer is to provide desired output by selecting the input signals given to it. This is done using the 2 input signals given as the select lines to it.

i) *Stage 1 – Standard 5MR with Additional Logic*

In this architecture 5 out of 7 is used an input to this 5MR as shown in Figure 3. A 5MR circuit is used to provide high output if there is any low in two of the five inputs. The decoder circuit is used to provide high output if there is any low in one of the five inputs and if all input is high. The schematic for this decoder is obtained from the Boolean expression as in equation (1) and the decoder circuit is shown in Figure. 4.

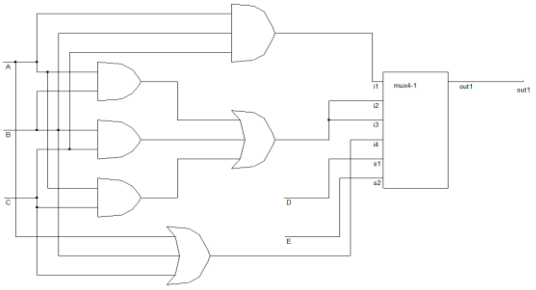

Figure3. 5 MR circuit.

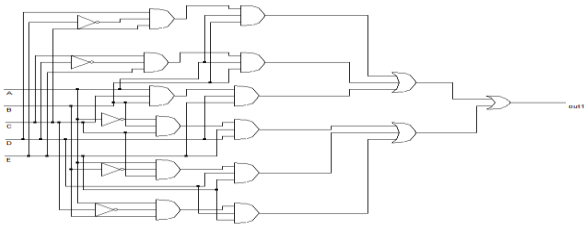

Figure 4. Decoder circuit

out1=ABCDE+A'BCDE+AB'CDE+ABC'DE+ABCD'E+ABCDE' (1)

In addition to the 5MR system, a combinational logic circuit is developed which is used to provide high output if there is any low in two of the five inputs for the conditions which is not met in 5MR system as in Figure 5. The equation (2) conveys the Boolean expression for this module.

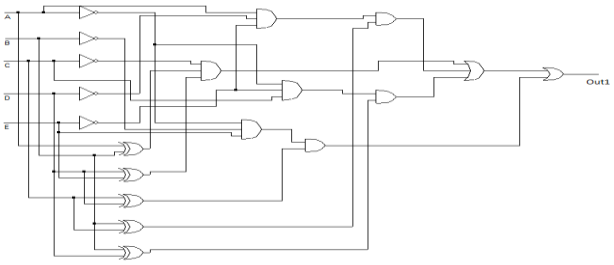

Figure-5. Combinational circuit – I.

out1=(A⊕B)(D⊕E)C' + (C⊕D)A'B'E + (B⊕C)AD'E' + (B ⊕D)A'E'C (2)

ii) *Stage 2 – Multiplexer With Combinational Logic*

The output of previous stage, i.e. 5MR and Combinational logic are combined using an OR gate. This is given as input to MUX along with decoder output. Input signals F and G are given as select lines to MUX. Thus the output of the multiplexer gives the required result..

iii) *Modified 7MR structure*

The said two stages are combined serially to construct a modified 7MR structure. This structure gives a clear insight of the usage of the 5MR circuit, Combinational circuit and the decoder circuit, giving intricate details about the entire structure. The modified 7MR schematic is shown in Figure 6.

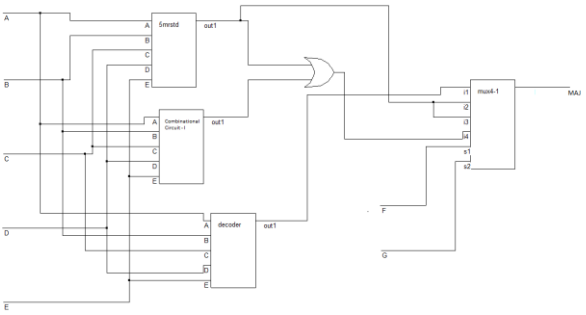

Figure-6. Modified 7MR schematic with 5MR.

B. *Modified 7MR using 3MR(Architecture II)*: This architecture also consists of 2 stage system. The first stage contains standard 3MR and a combinational circuit. The second stage involves use of a 16x1 multiplexer. Here we are using more input signals as select lines, we need a 16x1 multiplexer.

i) *Stage 1 – Standard 3MR with Additional Logic*

Here 3 out 7 inputs are given as input to 3MR. A 3MR circuit is used to provide a high output if there is any low in one of the three inputs, i.e. it can tolerate only one error. This is shown as schematic as in Figure 7.

The combinational circuit – II is used to realize the additional logic that is left after realizing the 7MR truth table using 3MR logic as in equation (3). The schematic for this combinational circuit is shown in Figure 8.

$$out1 = (A \oplus C)\, B' + A'BC' \qquad (3)$$

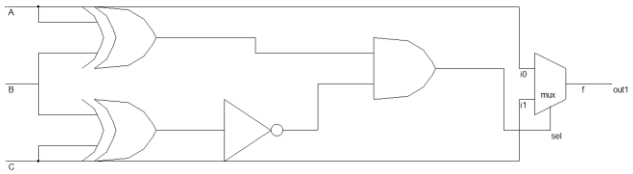

Figure7. 3MR circuit.

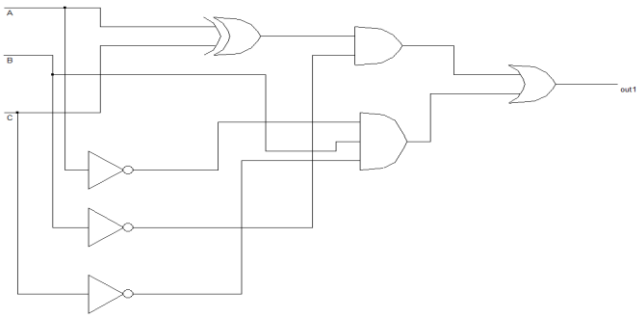

Figure8. Combinational circuit – II

ii) *Stage 2 – Multiplexer With Combinational Logic*

The output of the standard 3MR circuit and Combinational logic-2 is combined together using OR gate and is fed as input to 16x1 multiplexer as input. Input signals D, E, F and G are given as select lines to MUX.

iii) *Modified 7MR structure-2*

The aforementioned stages are combined together and the final output is got from the 16-to-1 multiplexer. The various inputs to the MUX are shown in the schematic. The modified 7MR schematic is shown in Figure 9.

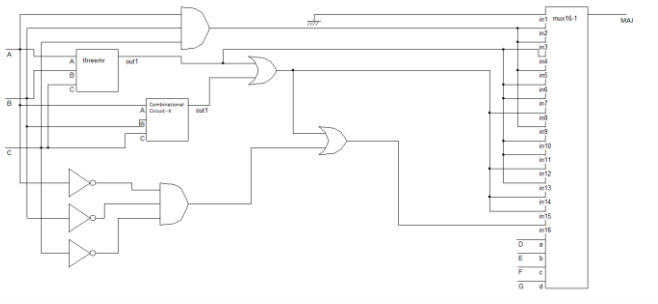

Figure9. Modified 7MR schematic .with 3MR.

C. Modified 7MR using full adder(Architecture III)

This Architecture was developed using the principle of Carry and Sum generation of Full Adder Circuits. The structure is developed by using two full adders and the subsequent decoder logic to decode the output of the full adder to result in the desired output. The full adder schematic is shown in Figure 10.

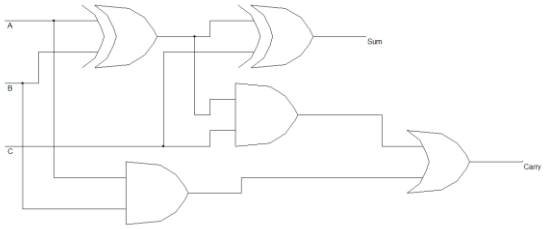

Figure10. Full Adder Circuit.

The additional logic is designed to combine the 4 output signals of the 2 Full Adder circuits and 1/7 input signal to give the desired result. The error recognition at the output of each full adder is given by the following:

i) 0 errors at input; Sum=1, Carry=1.

ii) 1 error at input; Sum=0, Carry=1.

iii) 2 errors at input; Sum=1, Carry=0.

iv) 3 errors at input; Sum=0, Carry=0.

The modified 7MR using full adder is shown in Figure 11.

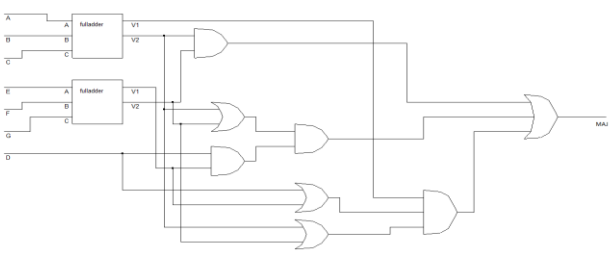

Figure11. Modified 7MR schematic. With Full Adder.

IV. Simulation Results

The ECAD tools like DSCH and Micro wind are used to obtain simulation results in this study. The Micro wind is a layout editor tool used to generate a layout by means of compiling Verilog hardware description language (HDL)[11,12]. This HDL is generated using DSCH tool for the given schematic; this DSCH is a schematic editor tool. The power dissipation, critical path delay, and layout area simulation results are obtained as in Table 1.

Table1. Simulation results with 120 nm technology.

Design Type	Surface Area (μm^2)	Power (mW)	Delay (ns)	Number of Transistors	Figure of Merit $\times 10^4$
Existing	2421.9	0.195	0.930	268	22.76
7MR using 5MR	2398.0	0.148	1.000	328	29.57
7MR using 3MR	3924.8	0.036	1.23	188	57.5
7MR using full adders	962.2	0.049	0.695	112	305.17

The 7MR using full adders obtain better results as compared with the existing 7MR and other architectures; this schematic obtains 962.2 μm^2 area, 0.049 MW power dissipation, and 0.695 ns critical path delay. The reciprocal of the product of area, power, and delay is calculated as FOM for better comparison. The modified 7MR using full adders obtain a higher FOM as 305.17 as compared with other designs. The hardware implementations with FPGA are obtained in Table 2 with resource utilization report as number of logic elements, critical path, and power dissipation. The delay is calculated using Time Quest Timing analyzer the power dissipation results are obtained using power play analyzer tool for comparisons. The reciprocal of the product of power, delay, and area is referred here as the figure-of-merit (FOM). This FOM performance metric would help us to find the optimum design among all[13].

Table-2. FPGA implementation results.

Benchmark circuits	Design type	Power (mW)	Critical delay (ms)	No. of Logic Elements
74182(4-bit Carry Look Ahead Generator)	Existing 7MR	138.96	15.918	62
	7MR using 5MR	143.16	15.038	75
	7MR using 3MR	142.97	16.498	59
	7MR using full Adder	143.26	24.450	59
74283(4-bit Adder)	Existing 7MR	135.29	19.397	101
	7MR using 5MR	140.58	19.188	122
	7MR using 3MR	143.45	14.890	105
	7MR using full Adder	143.24	14.288	97
74L85 (4-bit Magnitude Comparator)	Existing 7MR	131.84	14.502	99
	7MR using 5MR	130.81	15.354	131
	7MR using 3MR	132.16	15.671	118
	7MR using full Adder	135.05	15.941	86
C17	Existing 7MR	132.80	11.364	27
	7MR using 5MR	130.81	12.216	24
	7MR using 3MR	129.90	12.216	24
	7MR using full Adder	131.35	12.216	24

In the Table 2, the modified 7MR using full adder obtain 131.35 MW power, 12.216 ns delay, and contains 24 logic elements for the ISCAS'85 benchmark circuit (C17). Similar kind of results are obtained for the 74LX circuits; 74182, 74283, and 74L85 which are 4-bit carry-look ahead generator, 4-bit adder, and 4-bit magnitude comparator respectively. Table 3 contains simulation results using Micro wind for various nanometer technology processes[14-16].

Figure 12 shows the Simulated Output for Modified 7MR Architecture. This Architecture is the one which uses full adder in the circuit design. The figure is basically a timing diagram and shows output waveform for different inputs to the circuit. There is a delay in the output waveform as it shows the output for the previous inputs.

Table-3. Microwind tool results with 120 nm, 90 nm, and 70 nm.

Design	Metric	120 nm	90 nm	70 nm	No. of transistors
Existing 7MR	Delay (ns)	0.202	0.141	0.164	268 (134 nMOS, 134 pMOS)
	Area (μm^2)	2421.9	1681.9	1076.4	
7MR using 5MR	Delay (ns)	0.146	0.106	0.111	328 (164 nMOS, 164 pMOS)
	Area (μm^2)	2398.0	1665.3	1065.8	
7MR using 3MR	Delay (ns)	0.036	0.028	0.017	188 (94 nMOS, 94 pMOS)
	Area (μm^2)	3924.8	2725.5	1744.3	
7MR using full adders	Delay (ns)	0.024	0.021	0.014	112 (56 nMOS, 56 pMOS)
	Area (μm^2)	486.7	338.0	216.3	

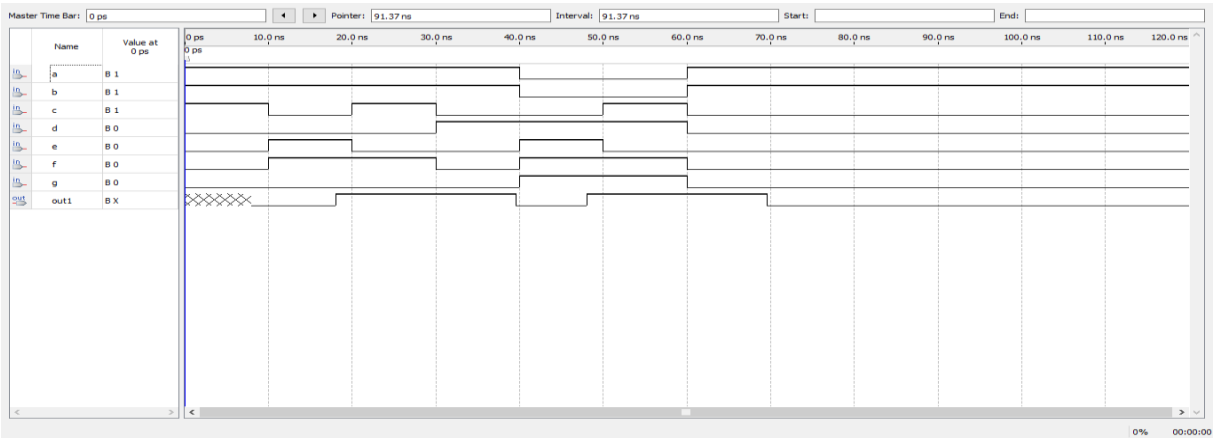

Figure-12. Simulated Output of Modified 7MR Architecture.

V. Conclusions

The fault-tolerant system design plays a vital role in the field of applied science and engineering. The hardware redundancy techniques are implemented here to improve the reliability. This study demonstrates various 7MR

architectures with comparative simulation results to choose a optimum design for practical applications. Since the power (P), area (A), and delay (D) should be minimized for a good design, the reciprocal of the product (PDA) which is the FOM would be higher. The proposed schematics are implemented on Alter a DE2-FPGA with industry standard benchmark circuits and the comparative simulation results analysis is done in detail. This work further can be extended to adopt hybrid redundancy with NMR architectures.

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