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A COMPARATIVE STUDY ON CMOS MAJORITY VOTER CIRCUITS USING MICROWIND

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Abstract

Objectives: With the development in technology, and the heavy dependence on it for pursuing day-to-day activities, this has arisen the need for the microelectronic technology used to be made redundant wherever necessary so that the regular activities are not affected.

Methods/Statistical analysis: Triple-modular redundancy (TMR) uses a voting scheme where there are three modules of the original system and even if one of the modules fails, the other two can maintain the integrity of the system and produce a fault-free output. ECAD tools like Microwind2.6a and DSCH2.6c is used.

Findings: With the various voter circuits using different gates and CMOS transistors, a SET tolerant voter circuit is obtained with different values of figure of merit, depending on the context where the voter is used, one among the different voters could be used for fault-tolerance.

Application/Improvements: SET tolerant systems can be particularly useful where, relatively little circuit redundancy can be afforded to achieve a better reliability like space, avionic, military and banking systems.

Keywords: Fault-tolerant, majority voters, single-event effects(SEE), single-event transient (SET), triple modular redundancy (TMR), VLSI.

1. Introduction

In the current age where the dependence on the microelectronic circuits has increased manifold, there exists a need for reducing or if possible, eliminate the possibility of failure of those circuits[1]. This has given rise to the need for research on increasing the reliability of those systems[2]. Mission and safety critical applications must be fault-tolerant at all times[3]. For example, the military, banking, space, avionic, transport systems, etc[4].

Faults in a microelectronic device could occur due a phenomenon called as single-event effects (SEE)[5]. When a single ionizing particle (ions, electrons, photons) strikes a sensitive node of a microelectronic device such as microprocessor, semiconductor memory, or power transistors, then there is an irrevocable change of state of the output of the device[6,7]. This is called as single-event upset (SEU). When this SEU propagates through a circuit, it is considered as single-event transient (SET)[8,9]. SEE like SEU and SET must be tackled for a system to be self-tolerant. SEU is also called as soft error[10,11]. TMR (Triple-Modular Redundancy) and modified TMR can be used to achieve this[12]. TMR is a voting based system, where in if when one of three system fail, the other two systems can correct and mask the fault[13]. TMR can particularly be helpful wherein there is a need for a circuit to virtually have no margins of error[14,15]. This study deals with proposing an efficient, fast and a reliable TMR voter scheme and also provides a comparative study of various other voter schemes[16,17]. This study is organized as follows. Section II provides an insight to the various schemes of majority voters computation using nMOS and pMOS transistors. Section III describes the different mirror circuits which could be used a majority voter. Section IV and V provides the simulation results as obtained from the ECAD and also a comparative study of the various majority voter schemes described in the previous sections and Section VI concludes the study.

2. Voters using MOS and p MOS Transistors

This section produces various voter circuits to compute the majority using nMOS and pMOS transistors. Some circuits are also constructed using the pass transistor concept. The circuit performance is determined depends on the number of transistors which reflects the area and number of nodes interconnected which reflects the power and delay.

2.1 12 Transistor implementation

The majority is computed here as the carry out of a full adder using nMOS and pMOS transistors. The carry out is computed as in Equation (1),

$$C_{out} = AB + BC + CA \quad (1)$$

The transistor level schematic using the above Equation is shown in Figure1. This is referred as "Ckt1" which would be easy for a comparative study at the end among all the other circuits.

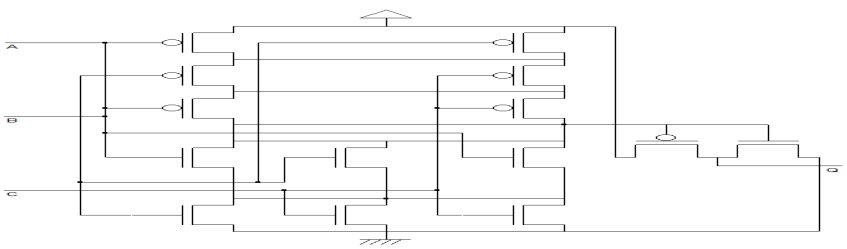


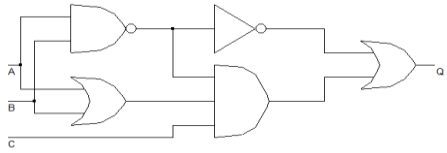
Figure 1. 12 Transistor implementation (Ckt1).

2.2 Using carry out of a full adder

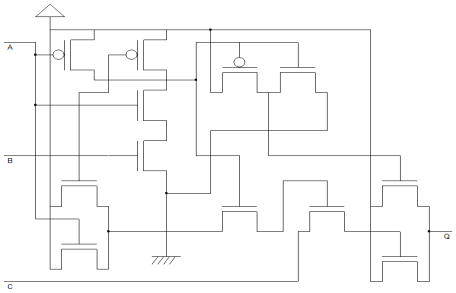
The carry out of a full is computed using AND, OR, Inverter gates as in Equation (2),

$$\text{Maj} = C_{out} = (\overline{AB}(A+B)C)+AB \tag{2}$$

The transistor level schematic based on this Equation is referred as "Ckt2" and shown in Figure 2a. The corresponding transistor level schematic is shown in Figure 2b.



(a)



(b)

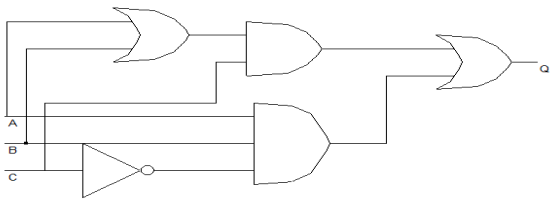
Figure 2. Ckt2 using (a) logic gates and (b) transistors.

2.3 Majority computation using AND, OR, and Inverter gates

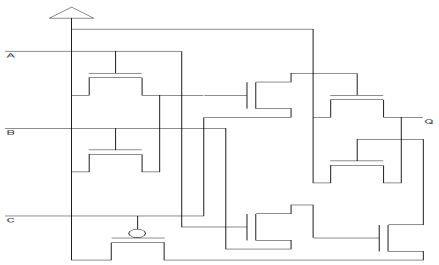
The majority can also be computed using AND, OR, and Inverter gates as in Equation (3),

$$\text{Maj} = C_{out} = (\overline{C}(AB))+(C(A+B)) \tag{3}$$

The transistor level schematic based on this Equation is referred as "Ckt3" and shown in Figure 3a. The corresponding transistor level schematic is shown in Figure 3b.



(a)

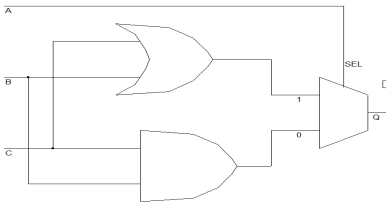


(b)

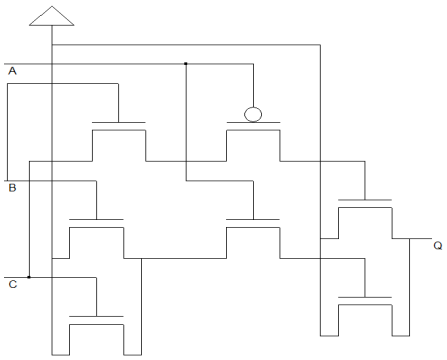
Figure 3. Ckt3 using (a) logic gates and (b) transistors.

2.4 Majority computation using Mux, OR, and AND gates

If the input A = 0, then the majority is computed as "BC". If the input A = 1, then the majority is computed as "B+C". The transistor level schematic based on this concept is referred as "Ckt4" and shown in Figure 4a. The corresponding transistor level schematic is shown in Figure 4b.



(a)

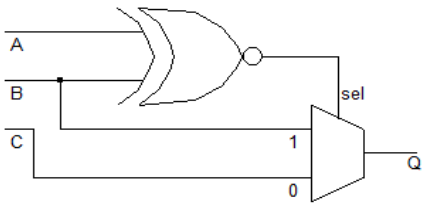


(b)

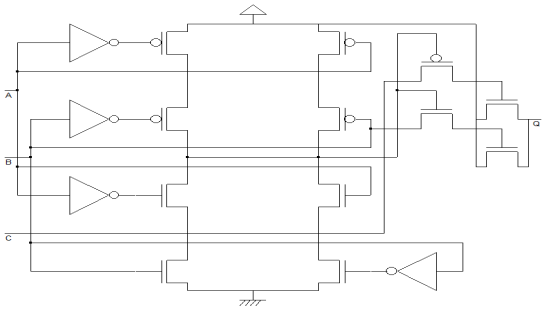
Figure 4. Ckt4 using (a) logic gates and (b) transistors.

2.5 Using Mux and ExOR gates

If the inputs A = B, then the majority is determined as "B". If the inputs A and B are not equal, then the majority is determined as "C". The transistor level schematic based on this concept is referred as "Ckt5" and shown in Figure 5a. The corresponding transistor level schematic is shown in Figure 5b.



(a)

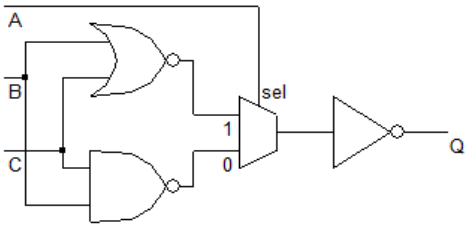


(b)

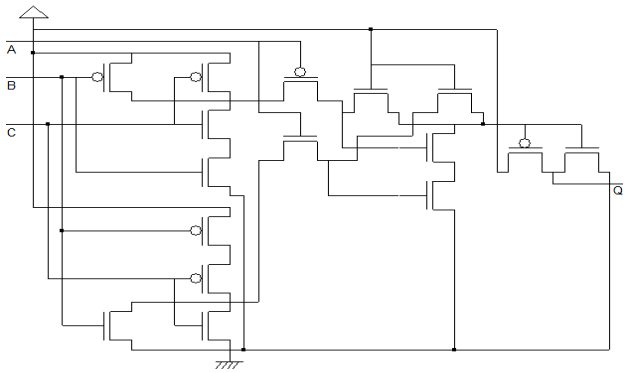
Figure 5. Ckt5 using (a) logic gates and (b) transistors.

2.6 Using Mux, NOR and NAND gates

The majority computation is also calculated using Mux, NOR, and NAND gates as in Figure 6a. This is referred as "Ckt6" and the transistor level schematic is shown in Figure 6b.



(a)



(b)

Figure 6. Ckt6 using (a) logic gates and (b) transistors.

2.7 Using Manchester carry chain adder concept

The carry out of a full adder is determined here using the Manchester carry chain concept and is shown in Figure 7. This circuit is referred as "Ckt7".

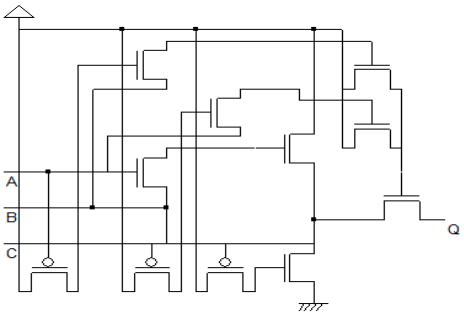


Figure 7. Carry out using Manchester carry chain (Ckt7).

2. Voters using mirror circuits

This section discusses the voter circuits implementation using the concept of mirror circuits. In the conventional CMOS circuits, if the nMOS transistors are connected serially then the corresponding pMOS transistors will be connected parallel, and vice versa. Here, the propagation delay from high-to-low (t_{pHL}) and low-to-high (t_{pLH}) would differ in the way the transistors are connected. But in the mirror circuits, if the nMOS transistors are connected serially,

then the corresponding pMOS transistors are too connected serially. Similarly, if the nMOS transistors are connected in parallel, then the corresponding pMOS transistors are too connected in parallel. So the delay would be symmetric, i.e., the t_{pHL} would be equal to t_{pLH} and vice versa.

3.1 Conventional mirror circuit

The majority computation is done here using the conventional mirror circuit using the carry out of a full adder. Since the truth table of full obeys the principle of mirror concept, this can be achieved. For example, if $A=B=C_{in} = 0$ then the Cout = 1 and if $A=B=C_{in}=1$ then $C_{out} = 1$. Figure 8 shows the voter circuit using this mirror concept and is referred as "Ckt8".

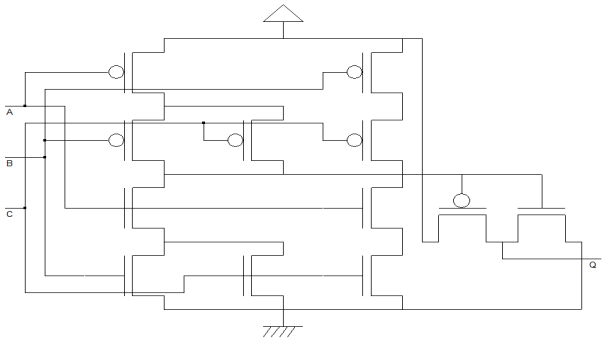


Figure 8. Voter circuit using conventional mirror (Ckt8).

3.2 Voter using XOR mirror

The XOR gate obeys the principle of mirror concept. For example, if A=B=0 then the output of XOR is 0 and if A=B=1 then the output is also 1. Here, the majority is computed using this XOR mirror concept and is shown in Figure 9. This is named here as "Ckt9".

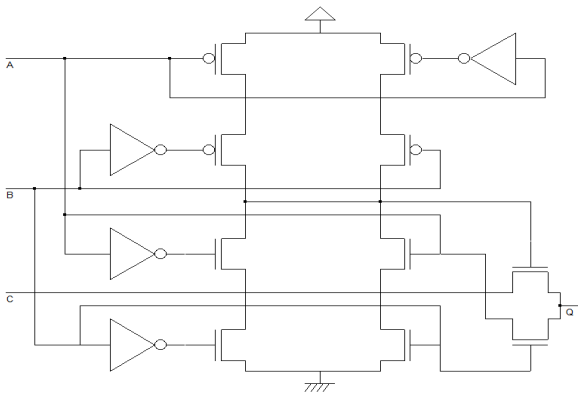


Figure 9. Voter circuit using XOR mirror (Ckt9).

3.3 Voter using XNOR mirror

Similarly, the voter is designed using XNOR mirror concept and is shown in Figure 10 and the this is referred as "Ckt10".

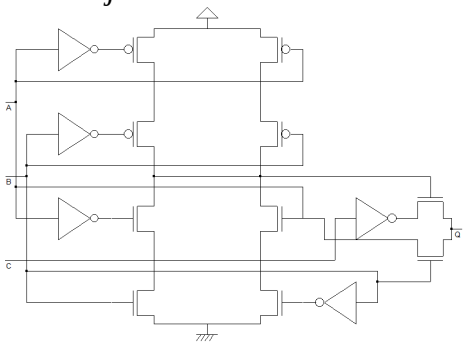


Figure 10. Voter circuit using XNOR mirror (Ckt10).

3. SIMULATION RESULTS AND DISCUSSION

The simulation results are obtained for the Section II circuits and the Section III circuits which includes power, area, and delay using DSCH and Micro wind tools [18,19]. The figure-of-merit (FOM) is obtained by determining the reciprocal of the product of power, delay, and area for the 120 nm technology. Table 1 produce simulation results for the Section II circuits. It shows that "Ckt2" produces a better FOM as 425.7 as compared with others. It is apparent that "Ckt3" obtains less power as 3.435 µW and lower delay as 0.420 ns. The Table 2 and Table3 obtains simulation results for 90 nm and 70 nm process technology respectively.

Tables 4 to Table 6 obtain simulation results of the Section III circuits. It is apparent from Table 4 that the "Ckt8" produce a better FOM as compared with others in 120 nm process technology. Here, the "Ckt8" offers a low power dissipation and lower area as 108 µW and 187.2 μm^2 respectively. The "Ckt9" produces a lower delay as 0.720 ns as compared with others.

Table1. Simulation results of voter circuits (Section 2 circuits) with 120 nm.

Metrics	**Ckt1**	**Ckt2**	**Ckt3**	**Ckt4**	**Ckt5**	**Ckt6**	**Ckt7**
Power (µW)	92.845	5.633	1.130	**1.047**	8.991	8.022	48.915
Delay (ns)	1.100	1.370	**0.440**	0.580	0.750	0.580	2.480
Area (µm2)	248.1	190.5	186.2	243.0	247.0	**97.3**	178.4
No. of transistors	14	12	8	**7**	20	30	11
FOM $\times 10^5$	6.611	68.02	**1080**	677.6	300.1	220.89	4.67

Table 2. Simulation results of voter circuits (Section 2 circuits) with 90 nm.

Metrics	**Ckt1**	**Ckt2**	**Ckt3**	**Ckt4**	**Ckt5**	**Ckt6**	**Ckt7**
Power	71.27	3.874	**0.675**	0.676	6.745	4.370	19.91

(µW)	1						2
Area (µm2)	172.3	132.3	126.8	168.8	171.5	**67.6**	123.9

Table 3. Simulation results of voter circuits (Section 2 circuits) with 70 nm.

Metrics	**Ckt1**	**Ckt2**	**Ckt3**	**Ckt4**	**Ckt5**	**Ckt6**	**Ckt7**
Power (µW)	80.113	3.474	**0.754**	0.761	6.221	3.938	7.501
Area	110.2	84.7	81.1	108.0	109.8	**43.3**	79.3

Table 4. Simulation results of voters (Section 3 circuits) with 120 nm.

Metrics	**Ckt8**	**Ckt9**	**Ckt10**
Power (µW)	**9.919**	13.574	252
Delay (ns)	2.580	**0.580**	**0.720**
Area (μm^2)	**213.8**	1314.1	251.0
No. of transistors	**12**	32	15
FOM $\times 10^5$	**18.27**	9.665	2.195

Table 5. Simulation results of voters (Section 3 circuits) with 90 nm.

Metrics	**Ckt8**	**Ckt9**	**Ckt10**
Power (µW)	**8.026**	8.308	181
Area (μm^2)	**148.5**	912.6	174.3

Table 6. Simulation results of voters (Section 3 circuits) with 70 nm.

Metrics	**Ckt8**	**Ckt9**	**Ckt10**
Power (µW)	6.541	5.723	**0.252**
Area (μm^2)	**95.0**	584.1	251.0

5. Conclusion

Since the reliability issue is an important concern nowadays, fault-tolerant circuit design is playing a vital role in the field of microelectronic circuits and systems. In a fault-tolerant circuit design, the correct response is expected even if any fault is occurred. This fault can be masked by implementing the hardware redundancy method like TMR. In TMR configuration, in addition to the original function module, two more copies of the original function modules referred as redundant modules are placed. Due to the redundancy, if one fault is occurred, this is masked by the redundancy technique through determining the majority among the three inputs. This study demonstrates various voters using the full adder circuit concept and mirror circuits too. The sole objective of VLSI design to optimize the power, delay, and area parameters to a lower value. But in some cases, a circuit may offer low power dissipation at the cost of performance or layout area and vice versa. So, this study analysis with different voters would be useful for the designers to choose the optimum one depends on the context.

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