ISSN: 0975-766X
CODEN: IJPTFI
Available Online through *Research Article*
www.ijptonline.com

RELIABILITY IMPROVEMENT BY HARDWARE REDUNDANCY USING ALTERA DSP BUILDER

Golla Akhila Sai Durga[1], Nuthalapati Divyasree[1], K Narasimhan[2], V Elamaran[2], Har Narayan Upadhyay[3]
[1]Dept., of ECE, School of EEE, SASTRA University, Thanjavur, India.
[2]Assistant Professor, Dept., of ECE, School of EEE, SASTRA University, Thanjavur, India.
[3]Associate Dean, Dept., of ECE, School of EEE, SASTRA University, Thanjavur, India.
Email: akhila.golla12@gmail.com

Received on: 19.10.2016 *Accepted on: 20.11.2016*

Abstract

Background/Objectives: In the current technology trend, the reliability plays a vital role especially in the mission critical applications like aerospace systems, defense communications, secure bank transactions, etc.

Methods/Statistical Analysis: The fault-tolerance techniques are needed for those applications since the cost is very high if they fail. In the past literature, the triple-modular redundancy (TMR) configurations are used and became popular to enhance the reliability of the system. This can be achieved using a voter circuit by calculating the majority among the three inputs.

Findings: This TMR configuration is implemented using Altera DSP builder as a case study. But if the voter fails, the TMR does not tolerate an error. This study analyze fault-tolerant voter circuit with 3-Modular Redundancy against single event transient (SET) errors. Some of the mostly used point processing algorithms like bitwise logical operation, negative image, and contrast stretching are used in this study; the high-pass filter is also implemented as a part of area processing algorithm to check the reliability with TMR configuration.

Application/Improvements: The FPGA resource utilization summary and the simulation results are obtained for various image processing algorithms using Quartus II 13.1 synthesis software.

Keywords: DSP builder; Fault-tolerant; Majority; Microwind; TMR; VLSI design; voting circuit.

Introduction

In the current microelectronics trend, due to the million transistors integration and the reduced size, the reliability is a major concern along with power and delay performance issues. For example, the replacement is not possible if the system or subsystems fail in aerospace applications [1]. Similarly, the banking systems should never halt; otherwise the amount of loss is huge. In defense communications, the security is a major problem if the message is corrupted or

lost. So the designers keep doing research on obtaining more appropriate fault-tolerant systems in their field of engineering [2]. The TMR systems are the most popular one to improve the reliability of a system. This TMR can tolerate one error at a time; if the tolerance is needed for multiple errors, then N-modular redundancy (NMR) configurations should be implemented. For example, the 5MR system can tolerate 2 errors; the 7MR system can tolerate 3 errors; the 9MR system can tolerate 4 errors. In general, the NMR system can able to tolerate (N-1)/2 errors if N is odd[3.] In this study, the hardware redundancy approach is implemented using Altera DSP builder tool as a part of verification of fault-tolerant technique. The image processing tasks are implemented easily using this tool with test images. Some basic tasks like bitwise XOR operation, negative image, and contrast stretching are done with TMR configuration. The Altera DSP builder is a tool through which the modules can be implemented on FPGA effectively. This study does also the synthesis work with Altera FPGA device along with compilation part of few image processing algorithms with hardware redundancy approach. The Xilinx System Generator (XSG) is an another popular tool to convert Matlab/Simulink blocks to synthesizable FPGA blocks. The system generator token in XSG converts these simulink blocks into Verilog or very high speed integrated circuits hardware description language (VHDL) code which can be synthesized using Xilinx ISE tool. This kind of hardware co-simulation is mostly used in a place where the fast prototyping algorithms is required [4,5.] The Altera DSP builder works in a similar way as Xilinx XSG does with Matlab/Simulink. The signal compiler is a component used for compilation and HDL code conversion. The converted code may not be the optimized one for a specific application. This study does only the compilation part instead synthesis with FPGA [6,7]. The reliability improvement of a system can be done also by using information redundancy, software redundancy, and time redundancy. In the case of information redundancy, the check bits are added along with the message bits to correct the errors The process or algorithm is repeated if any error occurs in the case of software redundancy. In time redundancy, The receiver may ask for retransmission if any error occurs. This study discuss in detail about the hardware redundancy and also with fault-tolerant voter circuit [8]. This study demonstrates few point processing algorithms like bitwise XOR, negative image, and contrast stretching with standard 'cameraman' test image. Point processing algorithms are much powerful in applications like image watermarking, steganography, denoising, and other image enhancement methods. The pixel-by-pixel approach would become easy for this study working with Altera DSP builder which is compatible with Matlab/Simulink blocks [9]. This study is organized as follows. The Section II demonstrates the above said point processing algorithms with TMR configuration. The Section III presents an Altera DSP builder implementation of a fault-tolerant voter circuit for

better reliability. Finally, the Section IV obtains simulation results with industry standard benchmark circuit for a fault-tolerant 5MR voter circuit; the discussions and future work are also included.

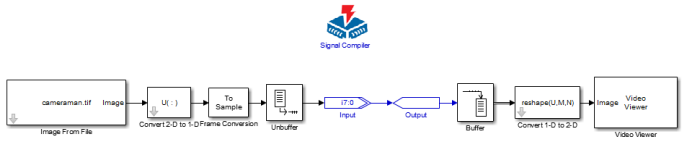
2. Point and Area Processing Algorithms

A. Bitwise XOR operation

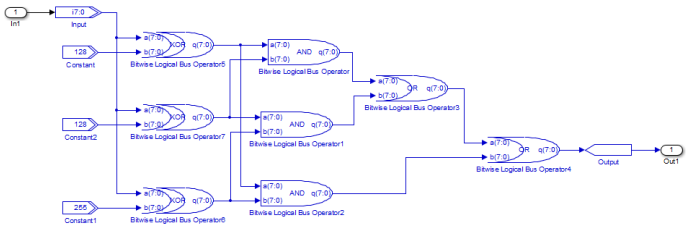
The first task of this study present a bitwise XOR operation which is shown in Figure 1. The pixel value 128 is added to the incoming pixels; the fault injection is done with adding 255 pixel value. In [10] This fault is masked by the TMR configuration and the resultant image is shown in Figure 2. The majority in TMR is calculated as in Equation (1),

$$\text{Majority} = AB + BC + CA \qquad (1)$$

where B, and C are the redundant function modules with original module A.



(a)



(b)

Figure. 1. (a) The complete system diagram. (b) TMR configuration. Figure.

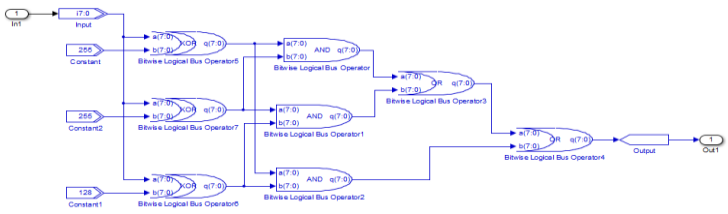
(a)

(b)

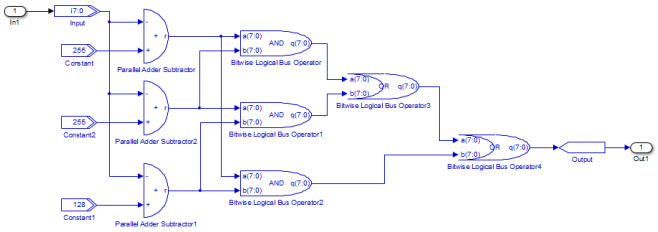
Figure. 2. (a) The input 'cameraman' image. (b) The resultant image.

B. Negative image

The bitwise XOR operation with 255 (all 1's) produce a negative image[10]. Also a negative image is obtained by subtracting the input pixel value from 255 value. This is done with TMR method which is shown in Figure 3; the compilation output of signal compiler is shown in Figure 4. The output negative image is shown in Figure 5.



(a)



(b)

Figure. 3. Negative image using (a) XOR with 255 and (b) 255 – input image.

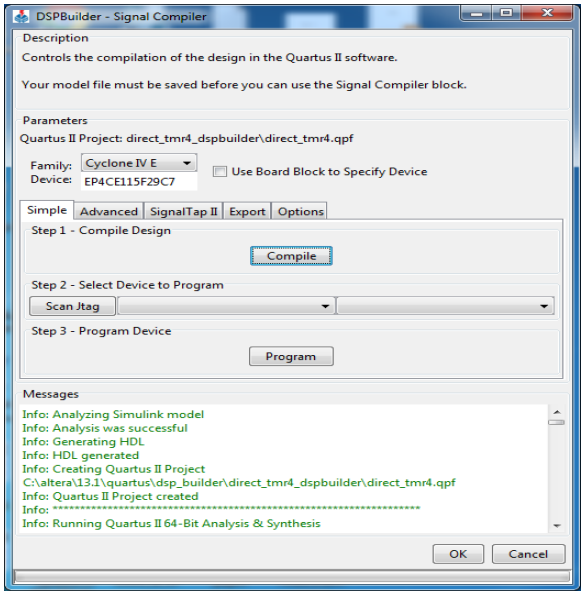
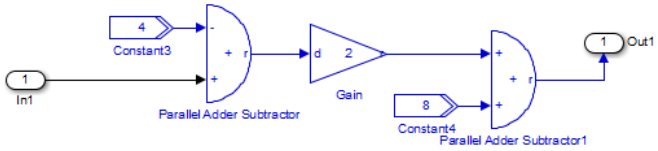


Figure 4. Signal compiler compilation output.

Figure 5. Negative image.



(a)

(b)

Figure-6. (a) Subsystem blocks of contrast stretching and (b) the output image.

C. Contrast stretching

The contrast stretching method is very often used to enhance the image[10] here, the following Equation (2) does this work and the corresponding Altera DSP builder subsystem blocks are shown in Figure. 6(a); the output image is shown in Figure. 6(b). This can be implemented in many ways depends upon the context and application.

output pixel = (12/6) (input pixel – 4) + 2 (2)

D. A 2x2 High-pass

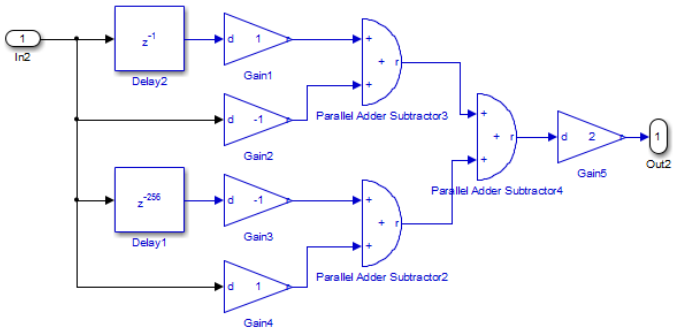
The edge detection is the mostly used technique in image enhancement algorithms[11] first, a 2x2 high-pass filter as in Equation (3) is implemented to obtain edges in an image. The corresponding Altera DSP builder blocks and the filtered images are shown in Figure 7a and Figure7b respectively.

$$\begin{bmatrix} 1 & -1 \\ -1 & 1 \end{bmatrix} \quad (3)$$

E. A 3x3 High-pass

This subsection demonstrates an edge detection using a 3x3 convolution mask as in Equation (4) which function as a high-pass filter [11]. The Altera DSP builder subsystems blocks are shown in Figure 8; the resulting image is shown in Figure 9.

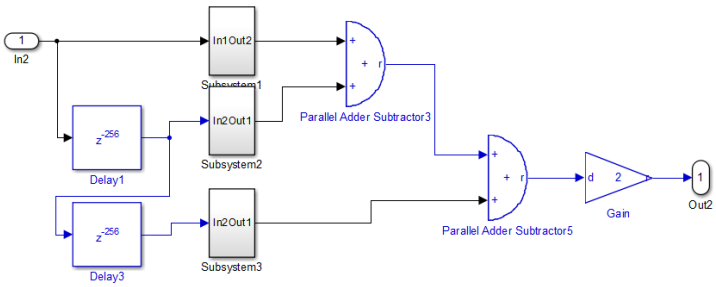
$$\begin{bmatrix} -1/9 & -1/9 & -1/9 \\ -1/9 & 8/9 & -1/9 \\ -1/9 & -1/9 & -1/9 \end{bmatrix} \quad (4)$$



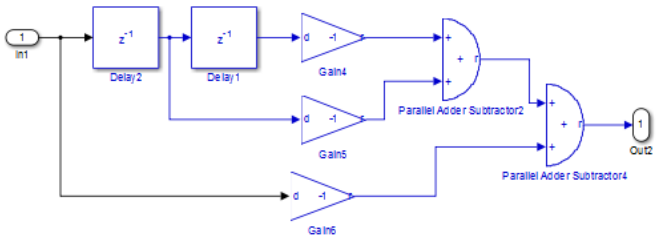
(a)

(b)

Figure 7. (a) Subsystem blocks of 2x2 high-pass filter and (b) the filtered image.



(a)



(b)

Figure. 8. Subsystem blocks of 3x3 high-pass filter.

Figure. 9. The filtered image.

3. Fault-Tolerant Voter Circuit

The fault-tolerant systems are handy in the mission critical applications mainly with a major concern with reliability. There are few applications where the reliability should be maintained perfectly throughout the operating times[12,13]. The TMR configuration helps to improve the reliability of a system using a voter circuit to compute the majority function. The majority computation part in a TMR plays a vital role to obtain an error free output [14]. If the voter circuit fails, there is no guarantee for a reliability of a system. That is in the voter circuit in TMR method, if any one of the 2-input AND gate or the 2-input OR gate fails, the result becomes incorrect and hence the reliability is poor [15]. So the fault-tolerant voter circuit is implemented in this study for better reliability with again a 3x3 high-pass filtering task and is depicted as in Figure 10. This circuit is organized in such a way that if any component fails, it produces a error-free output; this is robust against single event transient errors provided with reliable multiplexer block [16,17]. The corresponding Altera DSP builder implementation view is shown in Figure 11. The compilation report produced by Quartus II 13.1 synthesis software tool is shown in Figure 12.

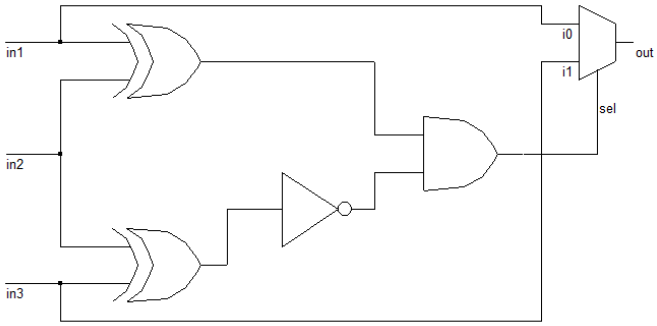


Figure. 10. The fault-tolerant voter circuit (Kshirsagar and Patrikar).

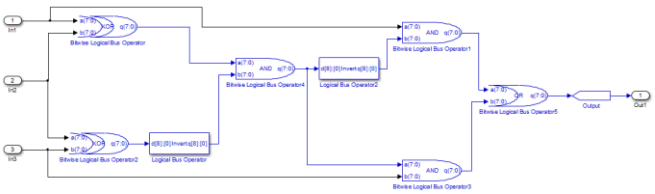


Figure 11. DSP builder subsystem blocks view.

Flow Summary	
Flow Status	Successful - Tue Mar 08 00:46:58 2016
Quartus II 64-Bit Version	13.1.0 Build 162 10/23/2013 SJ Full Version
Revision Name	direct_tmr141
Top-level Entity Name	direct_tmr141
Family	Cyclone IV E
Device	EP4CE115F29C7
Timing Models	Final
Total logic elements	240 / 114,480 (< 1 %)
Total combinational functions	181 / 114,480 (< 1 %)
Dedicated logic registers	207 / 114,480 (< 1 %)
Total registers	207
Total pins	18 / 529 (3 %)
Total virtual pins	0
Total memory bits	3,525 / 3,981,312 (< 1 %)
Embedded Multiplier 9-bit elements	0 / 532 (0 %)
Total PLLs	0 / 4 (0 %)

Figure 12. The compilation report.

4. Simulation Results

The resource utilization report is very often used as a performance metric while working with FPGA devices. This is done by calling Quartus II synthesis tool with compilation. The compilation report conveys the number of logic elements, total combination functions, total registers, total pins, and total memory bits used in the design circuit. The Table 1 obtains these results for the above said point processing and area processing algorithms. For example, a 3x3 high-pass filtering using TMR configuration with a fault-tolerant voter circuit obtains 240 logic elements, 181 combinational functions, 207 registers, 18 input/output pins, and 3525 memory bits.

Table 1. Resource utilization summary.

Design	Logic Elements	Combinational functions	Registers	Pins	Memory bits
Bitwise XOR	8	8	8	18	0
Negative image	8	8	8	18	0
Contrast stretching	83	61	72	18	1764
2x2 high-pass	83	61	72	18	1764
3x3 high-pass	240	181	207	18	3525
Fault-tolerant voter (3x3 HPF)	240	181	207	18	3525

5. Conclusions

This study demonstrated few important point image processing algorithms like point and area processes using Altera DSP builder tool with compatible Matlab/Simulink package. Then the system and subsystem blocks are converted to HDL code to implement the design on FPGA device. This kind of approach is more useful where the fast prototyping algorithms required. The fault-tolerant technique is combined with the image processing algorithms to check the reliability of a design mainly with TMR configuration which can tolerate one error. The error is injected in this study implicitly along with the input function modules to verify the fault-tolerant approach. This study further can be extended to N-modular redundancy (NMR) where N can be anything like 7, 9, 11, or more depends on the application to tolerate multiple errors.

Acknowledgment: We thank SASTRA University for providing financial support for this research work under the Research and Modernization fund – R&M/0034/SEEE-014/2013-14

References

1. Dubrova E. Fault-Tolerant Design. Springer, 2013.

2. Lala PK. Self-Checking and Fault-Tolerant Digital Design. Morgan Kaufmann publishers, 2001.
3. Koren I, Krishna CM. Fault-Tolerant Systems. Morgan Kaufmann publishers, 2007.
4. Navabi Z. Embedded Core Design with FPGAs. Mc-Graw Hill publishers, 2006.
5. Elamaran V, Hemavathy D, Jayapriya J, Upadhyay H N."Majority function computation using different voter circuits – a comparative study," in International Journal of Pharmacy and Technology, 2015,7(1), pp. 9764-9773.
6. Almukharizim S, Sinanoglu O, "A hazard-free majority voter for TMR-based fault tolerance in asynchronous circuits," in Proc. Des. Test Workshop, Dec. 2007, pp. 93-98.
7. Balasubramanian P, Maskell D L. "A distributed minority and majority voting based redundancy scheme," in Microelectronics Reliability, 2015,55(9-10),pp. 1373-1378.
8. Elamaran V, Upadhyay H N. "CMOS VLSI design of lo power SRAM cell architectures ith new TMR: A layout approach, " in Asian Journal of Scientific Research, 2015,8(4), pp. 466-477.
9. Elamaran V, Upadhyay H N. Low power digital barrel shifter datapath circuits using Microwind layout editor with high reliability, In: Asian Journal of Scientific Research, 2015,8(4), pp. 478-479.
10. Elamaran V, Rajkumar G. FPGA Implementation of Point Processes using Xilinx System Generator, In: Journal of Theoretical and Applied Information Technology, 2012, 41(2), pp. 201-206.
11. Chen C H, Quidwai U. Digital Image Processing: An Algorithmic Approach with Matlab. CRC press, 2009.
12. Crane R. A Simplified Appraoch to Image Procesing – Classical and Modern Techniques in C. Prentice Hall, 1997.
13. Amusan O A, Massengill L W. Single-event upsets in deep-submicrometer technologies due to charge sharing, IEEE Trans. Device Mater. Reliab., 2008,8(3), pp. 582-589.
14. Shooman M L. N-modular redundancy, In: Reliability of Computer Systems and Networks: Fault Tolerance, Analysis and Design. Wiley, 2002, pp. 145-201.
15. Huang C. Robust Computing with Nanoscale Devices: Progresses and Challenges. Springer, 2010.
16. Abraham J A, Siewiorek D P. An algorithm for the accurate reliability evaluation of triple modular redundancy networks, IEEE Trans. On Computers, 1974, 23(7), pp. 682-692.
17. Kshirsagar R V, Patrikar R M. "Design of a novel fault-tolerant voter circuit for TMR implementation to improve reliability in digital circuits," in Microelectronics Reliability, 2009, 49(12),pp. 1573-1577.