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DESIGN OF A 45nm LOW POWER COMPARATOR USING CMOS LOGIC

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Abstract

The aim is to give an improved Complementary Metal Oxide Semiconductor based comparator using a preamplifier-sequential circuit operated by a clock. Design is proposed to be implemented in Flash Analog-to-Digital Converter (ADC). The importance of this design is that it is proficient of operating at large frequency ranges and increase the performance of an analog to digital converter. The design is made in 45nm CMOS Technology.

Keywords: Digital comparator, N-mos transistor, P-mos transistor, clock, Flash analog to digital converter.

Introcution

A device that gives the comparison between two inputs either currents or voltages and gives digital signal as an output comparing which is larger. It has n input terminals that are analog and a digital output that gives binary bits. Comparators are generally operates fast these circuits are non resistive to the characteristic speed-power trade-off. High rate comparator devices use transistors with different configurations. So the power consumption of the devices will be high. Either a high rate comparator is made use or a low rate comparator is made used basing on application it is implemented for. In case of chip-scale packages and handy device applications we use nano-scale comparators.

i) Comparators in Analog-to-digital converters

When a comparator performs an operation if an input voltage is either minimum or maximum for a cut-off voltage, it is in effect with single-bit quantization. This operation is used in many analog to digital converters in amalgamation with other devices to accomplish n-bit quantization. Performance of a rigid voltage comparator will normally be better than a general-purpose Op-Amp which is used as a comparator. A voltage comparator may also contain added features like precision, domestic voltage reference, a variable triggered input structure. A voltage comparator is considered to interface of a digital logic periphery (CMOS). The output is digital state often used to the real life

applications to digital circuits like analog to digital converters for signal processing. If there is a stable voltage source, for instance, a DC regulating device in the data path, a comparator is just the corresponding to serial amplifiers. When the voltages are barely equal, the output voltage will not be into one of the logic levels, thus analog signals will enter the digital compatibilities with unexpected outcomes. To convert this range as minute as feasible, the series of amplifiers with high gain are implemented. The circuit comprises of mainly bipolar transistors. For large frequencies ranges, the input impedance of the stage is low. This minimizes the saturation, large bipolar transistors that would escort to high recovery times. It is found in binary logic designs get better operation considerably though the operation is still lagging that of circuits with amplifiers using analog signals. For applications in flash ADCs the circulated signal across the ports gives present gain and voltage gain when every electronic equipment and resistors then perform as mode-changers.

Project Description

B. Block diagram

Fig (i)

C. Working of Components in the block diagram

Since the design of a digital comparator is based on Complementary logic it consists of PMOS transistors and NMOS transistors and the input given is a triggered input from the clock and the output generated will be in digital form.

PMOS Transistor: P-type metal-oxide-semiconductor logic uses p-channel metal-oxide semiconductor transistors (MOSFETs) to implement logic gates and alternative digital circuits. PMOS semiconductor units operate by forming associate degree inversion in associate degree n-type transistor body. It consists of "source" and "drain" terminals. The p-channel is created by supply input voltage to the gate terminal. Like alternative MOSFETs, PMOS transistors have totally different regions of operation: sub threshold, active and speed saturation, reverse saturation. The p-type MOSFETs area unit cut in a very PUN network between the output of the gate and voltage provide, once a resistance is placed between the output of the gate and also the negative gate voltage. The circuit is designed in such the simplest way that if the specified output is high, then the Pull-Up- Network are going to be saturated, forming a path between the active provide and also the output. Wherever PMOS logic is straightforward to implement and manufacture, it's several flaws likewise foremost terrible bother long-faced by the look is

that there's DC through a PMOS gate once the Pull-Up-Network is active, that is, whenever the output is giant, that ends up in standing power dissipation even if the circuit is inactive. Also, PMOS circuits area unit long where as shift from most voltage to minimum voltage, once shift from minimum voltage to most voltage , the transistors provide low resistance, and also the electrical phenomenon charge at the output gather in no time. However the resistance between the output and also the negative provide is way larger, therefore the high-to-low shift takes longer. Employing a resistance of lower price can speed up the method however additionally will increase standing power dissipation.

ii. NMOS semiconductor unit. N-type metal-oxide-semiconductor logic uses n-type field result transistors (MOSFETs) to implement logic gates and alternative digital circuits. These nMOS semiconductor units perform by making associate degree inversion layer in a very p-type transistor body. This inversion layer, referred to as the n-channel, will conduct electrons between n-type "source" and "drain" terminals. The n-channel is created by giving voltage to the gate terminal. Like alternative MOSFETs, NMOS transistors have four regions of operation: sub threshold, active, reverse saturation and speed saturation. MOS stands for metal-oxide-semiconductor. The MOSFETs area unit n-type sweetening mode transistors, organized in a very manner specifically Pull-Down-Networks between the output of the gate and ground. A pull up is placed between the positive provide voltage and every gate output. Any gate, as well as the logical inversion, will then be applied by planning a mixture of parallel logic AND (or) logic OR series circuits, specified if the specified output for a selected combos of mathematician input values is false, the Pull-Down-Network are going to be active, that means that a minimum of one semiconductor unit is permitting a path flow between the bottom and also the output. This causes a drop over the load, thus provides an occasional voltage at the output, representing the zero. For associate degree instance, here may be a NOR gate applied in schematic NMOS. If the voltage at either input A or input B is high digital price (logic 1) true within the case, the actual MOS semiconductor unit provides a really low resistance between the output and also the ground, forcing the output to be low (logic 0) false within the case. Once each input A and input B has high input each transistors conduct, making terribly lower resistance path to ground. The sole case wherever the output created high is once each transistors area unit at rest, that happens only if each input A and input B area unit low. This is often used because the electrical converter stage of the CMOS.

Clocked signals: The clocked logic circuit needs 2 stages. the primary stage, once Clock rate is minimum is named the start up stage at that the clock circuits area unit setup, and therefore the second section, once Clock is

most, is named the raising stage. Within the startup stage, the output are high by default. The electrical condenser, that represents the load of this gate, becomes active. as a result of the semiconductor at very cheap is off, it's impractical for the output to be driven low throughout this section.

Working Principle: Comparator has no of inputs from 1 to n and the inputs are compared and the best output is given to the device. An additional and very useful logic of the circuit is that it gives most significant output of the Digital Comparator circuit. Digital or Binary Comparators are made up from standard AND, NOR and NOT gates that compare the digital signals present at their input terminals and produce an output depending upon the condition of those inputs.

D. Working of comparator

The transistor level schematic is designed by using CMOS logic. This consists of pull up network with PMOS transistors connected between Drain Voltage and GND. The entire process of designing the circuit is done using the cadence software. The circuit uses four PMOS transistors and five NMOS transistors including the tail transistors. Transistors are placed in serial and parallel connections are made using the wires and respective inputs and outputs are given. The circuit consists of three inputs namely CLK, input one and input two and two output 1 and 2 where input 1 and 2 are input at n and p nodes, and CLK is the input, output 1 and output 2 are outputs at n, p nodes.

The entire schematic is converted into a symbol which represents the circuit diagram. Now this symbol is used in the test bench construction to generate the required waveforms.

Features of digital comparator:

Low Vdd. It uses low power and its compatable with all the digital circuits. Minimum sized transistors The size of the transistors can be reduced into a very small transistors of small sizes. As the size of the transistor is minute and the complexity of the circuitry very less the speed of the comparator and device in which it is implemented high. High operating frequency and low output impedence. No compensation for current and offset voltage.

Conclusion

From this paper it is concluded that the design of a 45nm comparator that is presented gives an increased performance than other comparators in operating frequency and also it shows minimum input impedance and also it requires no compensation current. It has very small circuitry and complexity of the system is very minute on comparison with other comparators.

Minimal sized transistors are used in the circuitry. It requires a low input power supply (Vdd). The main benefit of this circuit is that it can be attuned with any of the digital circuits. It can be widely used in flash Analog to Digital Converters which are extensively used in mobile communications wireless digital data transfer.

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