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TYPES OF STRUCTURES AND ADVANTAGES OF FINFET

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Abstract:

A multigate transistor is introduced in order to overcome the difficulties in the planar CMOS transistor such as high power consumption, low speed of operation and scaling issues. FinFET is one of the multigate transistors. It provides a various range of improved parameters like speed of operation, less power consumption, and a better scalability during design. FinFET technology has entered the market with a large scope of improving the existing design standards. As the FinFET technology is continuously scaling down to 20nm perfect electrostatic integrity of the fin channel is degraded because of stronger Short Channel Effect (SCE). In this paper a review is done on characteristics of FinFET as well as the Fabrication process involved in developing a FinFET.

Keywords—FinFet,Multigate,CMOS

I. Background

FinFET technology has been born as a result of rapid increase in the levels of integration. Moore's law has held true for many years from the birth of integrated circuit technology. It tells that the number of transistors in a given area gets doubled every two years. To achieve large levels of integration in IC design, many parameters have changed. Basically the feature sizes have reduced to enable large number of devices being fabricated within a given area. However other factors such as line voltage and power Dissipation have reduced with increased frequency. There are limits to the scalability of individual devices as the level to integration increased the conventional process technology shrunk towards 20nm, at this particular size many device parameters cannot be achieved. So it was necessary to consider significant improvements in changing the transistor structure and fabrication techniques.

II. Introduction

As Nano technology has advanced in recent years, the density of the chip and operating frequency has increased. The increase in operating frequency is responsible for increased power consumption of devices. Nowadays power

dissipation is the major consideration in VLSI circuits, as the reliability of the device depends on power dissipation. So there is a need to design circuits with low power dissipation. Thus the main goal of VLSI design is to achieve performance in the available power budget. In 1990s UC Berkeley team led by Dr.Chamming Hu proposed a new structure for the transistor (FinFET) would reduce leakage current The FinFET is one of the low power devices at the circuit level. The FinFET is also known as double gate MOSFET. The drain of FinFET is raised like a fin like structure, thus the name FinFET. This method allows multiple transistors to share common gate thereby reducing the overall power consumption. In terms of its structure, it has a vertical fin on a substrate which is implemented between a larger drain and source area. The gate orientation is at right angles to the vertical fin. This gate structure provides improved electrical control over the channel conduction and it helps to reduce leakage current and overcome short-channel effects. FinFet technology will allow various chip manufacturers to develop ultra-powerful processors. Taiwan Semiconductor Manufacturing Company is one of the biggest contract chipset maker, is investing a lot of money on this technology as they have already progressed improvement in its 16nm FinFet chipsets. Many multinational companies like Intel and Samsung are investing billions of dollars on FinFET technology because it's power efficiency and superior processing power.

III.Finfet Characteristics

In this section we will review the electrostatic characteristics and also mobility variation with electric field. Figure 1 is simplified depictions of a planar FET and a FinFET respectively. In the planar FET a single gate controls the source-drain channel. Such a gate does not have good electrostatic field control away from the surface of the channel next to the gate, resulting in leakage currents between source and drain even when the gate is off. By contrast, in the FinFET the transistor channel is a thin vertical fin with the gate fully "wrapped" around the channel formed between the source and the drain. The gate of the FinFET can be thought of as a "multiple" gate surrounding the thin channel. Such a multiple gate can fully deplete the channel of carriers. This results in much better electrostatic control of the channel and thus better electrical characteristics.

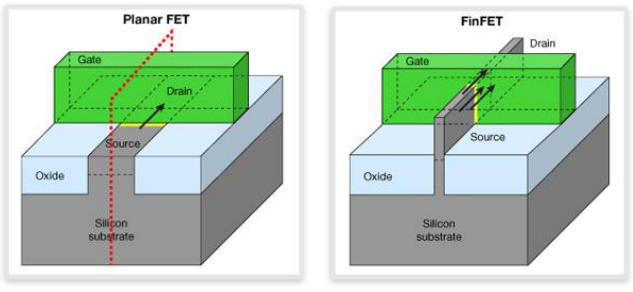

Fig 1: Planar FET and FinFET.

The Fig 1 displays the structural characteristic difference between a conventional planar FET and a FinFET. As we have specified earlier the gate of a FinFet is wrapped by a thin silicon "fin", the difference can be observed from the image clearly.

Transfer Characteristics of FinFet: Here the transfer characteristics are plotted for a Vd voltage of 0.05volts and 1Volts. This is generally considered to show the low power consumption used by FinFet.

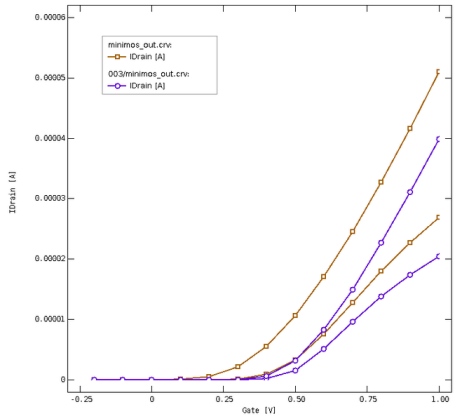

Fig 2: transfer Characteristics of a FinFet.

Gate leakage current with change in vdd:

The major characteristic of FinFET is less leakage current. The Fig 3 shows the gate leakage current for various vdd voltages. The graph is taken from global TCAD website.

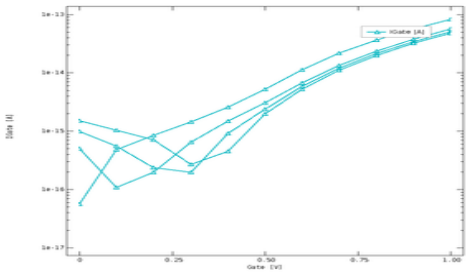

Fig 3: Gate leakage current w.r.t change in VDD.

IV. Various Architectures

Conventional FinFET have some disadvantages, so to overcome disadvantages like leakage currents, variation in threshold voltage (VTH), SCE etc. Some of the architectural variations have been done to the conventional FinFET to make the FinFET work more efficiently. In this paper some of the implemented architectural differences are reviewed.

Vertical Implantation to Form Self-Aligned Halo and Punch-Through Stop Pocket:

In this section Vertical Implantation to form self-aligned halo and punch-through stop pocket is discussed, referenced from a paper by Miao Xu[1]. The vertical implantation introduced in Bulk FinFET's. This method is used to form a

halo punch-through stop pocket (PTSP) at the same time, this formed halo and PTSP doping profiles will reduce the short channel effect and also reduce variations in VTH voltage. The Spacer-Image Transfer (SIT) method was implemented to form ultra-small fin structure (fin height~38nm, fin top width~9nm). The fins are fabricated with a relaxed pitch. The STI oxide provides the basic body isolation between adjacent fins while the transistors are still connected under the oxide. The formation of high dose junction implant at the base of the fin, Punch through Stop Layer (PTSL), is alternative way for the separation. It brings relatively low dopant in the channel region and avoids expansion of the depletion region to reduce the leakage between source and drain through the bottom part of fins without increasing integration complexity. As the FinFET technology is continuously scaling down to 20nm perfect electrostatic integrity of the fin channel is degraded because of stronger SCE. Normally halo and reverse halo implantations are used to control the SCE. A proper halo implantation in FinFETs will improve the SCE and reduce VTH scattering. The Fig 4 is taken as a reference from paper by Miao Xu[1].

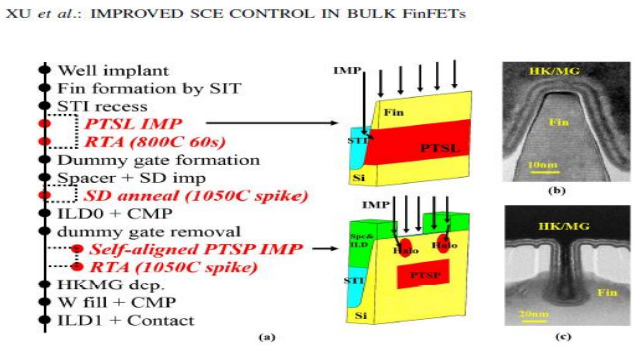

Fig 4: (a) The main fabrication process flow and sketch-maps of bulk FinFETs with conventional PTSL and proposed self-aligned Halo & PTSP implantation. The dashed lines are the distinction between the two implantation approaches. (b) The cross sectional view of fabricated Fin (Fin height ~38nm, Fin top width ~9nm). (c) The cross section view of gate profile (Lg ~25nm).

The Fig 4 shows the conventional PTSL and aligned halo & PTSP implementation. The figures (b) and (c) can be clearly compared where the PTSP pocket is clearly visible in the image(c).

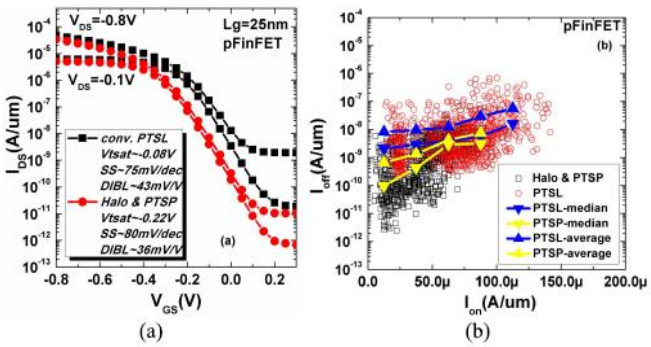

Fig 5: (a) IDS-VGS transfer curves of 25nm gate length HK/MG Bulk pFinFETs with conv. PTSL and self-aligned halo & PTSP doping structure. (b) On-off currents of conv. PTSL and self-aligned halo & PTSP devices.

The Fig 5 shows the characteristics of pFinFet with conventional PTSL and PTSP profiles. It is a plot of IDS-VGS transfer characteristics. Clearly the results show that the device with self-aligned halo and PTSP have much lower off currents than PTSL devices.

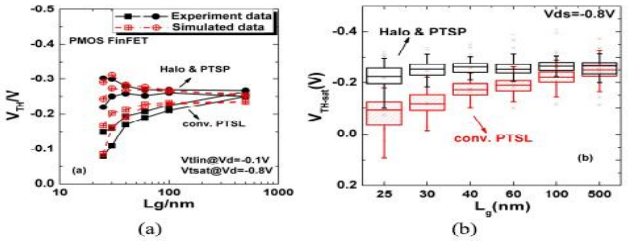

Fig 6: (a) VTH as a function of gate length for pFinFETs with conv. PTSL and self-aligned halo & PTSP doping structure. (b) Experimental data of VTH−sat variation vs. gate length.

The Fig 6 shows the comparison of short channel effect obtained for halo & PTSP and PTSL devices. Halo & PTSP doping profiles reduce the VTH−sat roll-off from 170 mV down to 30 mV compared with PTSL devices and exhibit behavior of Reverse Short Channel Effect (RSCE).

Using Germanium to model Industry standard FinFet:

In this section the review is done on a paper by Sourabh Khandelwal[1].In this paper an attempt is made to change the semiconductor material that is used in standard FinFETs. For this purpose, an industry standard FinFET model developed by Berkley University known as BSIM-CMG is considered. In this standard model germanium is added and results are obtained. The effect of perpendicular electrical field on hole mobility in germanium FinFETs is found to be different from silicon FinFETs. A separate mobility equation is taken into account and simulation is done from 130nm to 20nm technology. Germanium is mainly considered to be used in p-FinFET's since it has a high hole mobility. This work has been carried out in order to check whether industry standard BSIM-CMG model with silicon parameters can be used with upcoming Ge FinFets with accurate results.

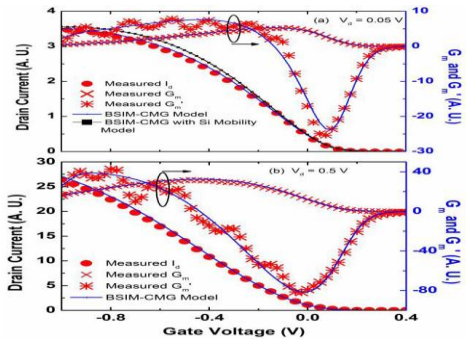

Fig 7. (a) Linear and (b) saturation region transfer characteristics of Ge p-FinFET data and BSIM-CMG model. The best model fits based on silicon mobility model is also shown in figure (a) for comparison. Gate-length is L = 130 nm and effective device width is 70 nm.

The above Fig 7 is taken as a reference from paper done by Sourabh Khandelwal[2] shows the modeling results for Ge-Finfets with gate-length L=130nm and width of 70nm with drain voltage Vd = -0.05v and saturation condition with Vd =-0.5v.

Fin shape impact on leakage:

In this section a review is done on Fin shape impact on leakage from a paper published by Brad D. Gaynor and Soha Hassoun [3]. In this paper a significant analysis is made to check the effect of "fin" shape on leakage current. It's been shown that for the first time "fin" shape significantly impacts transistor leakage in bulk tri-gate nFinFETs with thin fins when the fin body doping profile is optimized to minimize leakage. The main improvement made in "fin" design is that rectangular fin reduces the leakage current by 70%. Also the same fin shape can be implemented without increasing the chip area consumption. Using this method ultralow power nFinFETs with less than 1pA/μm can be designed.

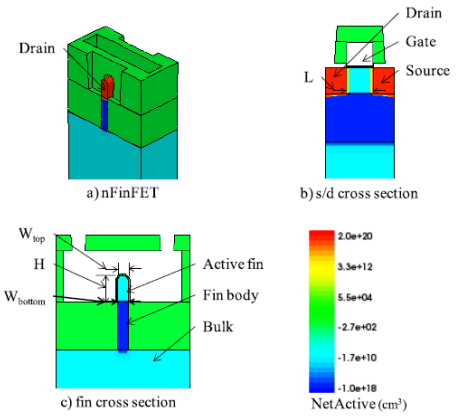

Fig 8: Doping concentration of nFinFET structure (a) isomorphic view, (b) source/drain cross section cut at the middle of fin, and (c) fin cross section cut at the middle of channel.

The Fig 8 shows the doping concentration of nFinFET structure isomorphic view. The source/drain cross section at the middle of "fin".

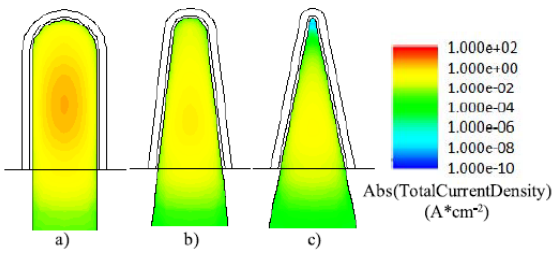

Fig 9: IOFF current density distribution of nFinFET with (a) rectangular fin cross section (*W*top = 15 nm), (b) trapezoidal fin cross section (*W*top = 7 nm), and (c) triangular fin cross section (*W*top = 1 nm), cut at the middle of channel. Rounded top corners with corner radius = *W*top/2, fin body doping concentration = 1e18 1/cm3.

The Fig 9 IOFF current distribution of nFinFET with rectangular fin cross section (Wtop = 15nm) and triangular fin cross section (Wtop = 1nm).

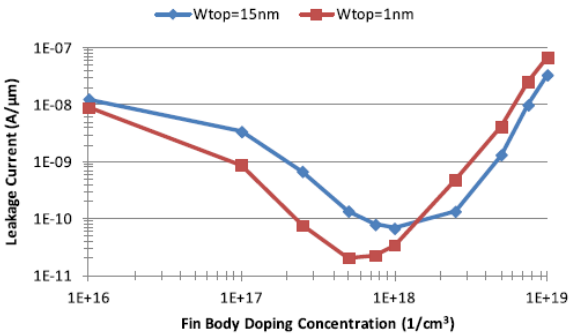

Fig.10: IOFF of rectangular and triangular nFinFET as a function of fin body doping. Active fin is undoped with concentration = 1e15.

The Fig 10 shows the leakage current comparison of rectangular fin (Wtop =15nm) and triangular fin (Wtop = 1nm) and doping concentration of 1/cm3. The Fig 8, Fig 9 and Fig 10 are taken as a reference from paper by Brad D. Gaynor and Soha Hassoun[3].

Optimization of pie-gate bulk FinFET Structure for logic operations:

In this paper a pie gate FinFET is implemented for logic applications which are suitable to be implemented in SoC's[4]. The influence of gate at bottom to junction depth, misalignment was examined for deeper junctions and shallower junctions. The characteristics of such bulk FinFET structure is analyzed by 3D device simulation and compared with SOI FinFET.

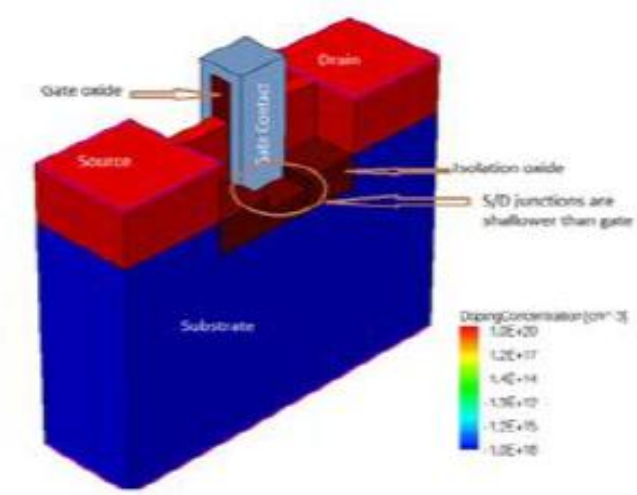

Fig.10: 3-D structure of FinFET

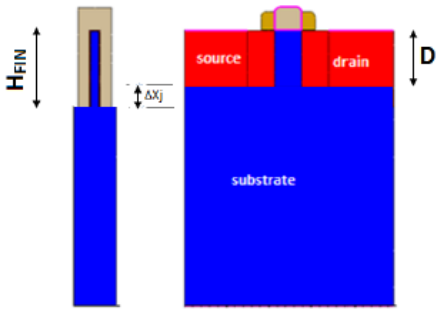

Fig.11: Cross-sectional view of pie gate FinFET structure.

The Fig 10 and Fig 11 show the cross-sectional view of general FinFET and pie gate FinFET. We can see that the gate structure of both the transistors differs. The pie gate FinFET offers better control over the channel than the conventional FinFET. The Fig 10 and Fig 11 are taken as a reference from paper by S L Tripathi[4].

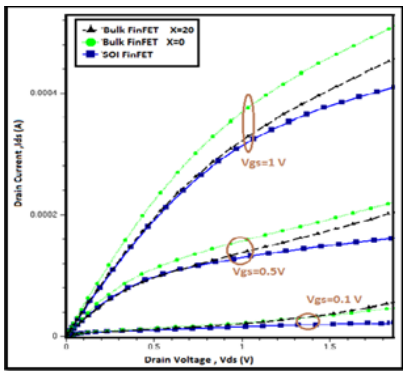

Fig.12: Output characteristics of different FinFET Structures.

The Fig12 shows the transfer characteristics of different FinFET's. From the Fig12 it can be seen that the threshold voltage varies for different configurations. Also the V_{DS} voltage varies for different configurations.

V. Advantages of Finfet:

Much lower power consumption allows high levels of integration. FinFETs require very less operating voltage there by reducing the overall power requirement. The static leakage current is reduced by 90%. The speed of operation is fast compared to conventional planar transistor.

Fig 3: Gate leakage current w.r.t change in VDD

VI. Conclusion:

This paper has reviewed on various structures of FinFET and their advantages. It's clearly seen that a generic FinFET model is not sufficient to implement an application altogether. Various alterations in the device structure has given much better results related to leakages, power consumption and short channel effects. So, before designing a circuit

or implementing a FinFET application one must carefully check the compatibility of the device with respect to their application. The clear cut understanding of the FinFET structure will give us better results. Many structural changes that are referenced in this paper are done to suit their application requirements.

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