DESIGN AND PERFORMANCE ANALYSIS OF LOW POWER HIGH SPEED FULL ADDER CIRCUIT FOR 1BIT, 8 BIT BY USING CMOS TECHNOLOGY

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Abstract

The full adder is the functional element of the digital systems. Basic arithmetic Operations like addition, subtraction, multiplication are done using full adders in digital systems. Addition is the basic arithmetic operation of multiplication performed using adder. Subtraction be performed by modifying the basic adder cell. Therefore performance of digital systems is improved by modifying the 1 bit hybrid full adder circuit which is the basic unit of the digital systems. Here we analysis the 1-bit hybrid full adder (14 transistors, 10 transistors, 8 transistors, 6 transistors) by using the techniques Gate diffusion technique, Modified gate diffusion technique and CMOS technique and 8 –bit hybrid full adder (14 transistors, 10 transistors, 8 transistors) by using ripple carry adder technique. We use the tools Digital schematic and Microwind tools.

Key words: Low power, Hybrid full adder, Cmos technology.

1. Introduction:

The development in electronics in recent days are more advanced not only in the size and weight but also in performance of the electronic item. The performance measures like power consumption, chip area, speed of operation should be considered by chip designer. The Arithmetic circuit plays important role in designing of the circuit .so the arithmetic circuit should have good performance characteristics, automatically the performance of electronic circuit can be increased. The full adder is the basic unit of the multipliers, digital signal processors, microprocessor and arithmetic related circuits. The chip should operate at low power and area required for designing of chip should minimum and operate at high speed. In designing of full adder we reduce the transistor count to reduce the chip area which leads to
reducing the performance of chip, voltage loss and driving capability is reduced. Some full adders are designed to reduce voltage loss in, transistors count, power consumption, delay time is reduced. Construction of multibit adder when they are connected in series is possible since the output driver for the full swing operation of the full adder is absent. Therefore many studies are made to get full swing voltage, output driving capability and power delay product. Therefore the goal is design a full adder with better performance and simple structure. In order to design a full adder with low circuit complexity, good circuit performance, modularized structures, a multiplexer based full adder is designed.

2. Related work:

In order to reduce the power consumption, layout area, delay, paratha Bhattacharya et al (2015) The 1 bit hybrid full adder design which employs both complementary metal oxide logic (CMOS) and transmission gate logic is proposed. The comparison is made with existing systems such as complementary pass transistor logic, transmission gate adder, transmission function adder, hybrid pass logic and so on. The tool used is cadence virtuoso tool in 180 nm or 90 nm technology.

Full adder is designed by using multiplexers and it is denoted as MUXFA. The MUXFA consists of three modules which deals XOR XNOR function, sum and carry function. Here the structure of multiplexer based full adder can be easily constructed by using single multiplexer module. The TSMC 0.18 µm CMOS technology is used

The low power CMOS full adder cells are designed by Hajar Zare Bahramabadi etal (2013). Here the XOR and XNOR logic gate architectures using pass transistor and transmission gate using 22 nm cmos technology.

The HSPICE simulator is used for obtaining simulation results. Here the 14 transistors hybrid full adder is designed.

GDI and pass transistors logic technique are proposed by Raj Kumar and Veerati Raju(2012).which are more power efficient than existing design technique Here only 10 transistor to design sum and carry functions. The tool used is cadence virtuoso in 180 nm technology.

Manoj kumar etal (2012) designed XOR gate by using three transistors but such type of design will have more noise margin of 2v with 3.3v input signals. XNOR module was also designed by addition of inverters which shows improvement is noise margin .i.e…. 3.2v.SPICE based on TSMC 0.35µm CMOS technology is used for designing the full adder.
3. Existing system: In full adder the primary operation is sum of operands a, b and carry input cin to obtain sum and carry. Performance of full adder is based on two factors they are circuit design techniques and the full adder logic architecture. The different types of logic architecture and circuit design technique are used to enhance the total performance in the full adder design approach.

The basic full adder logic architecture consists of three modules, Module I functions as XOR/XNOR gate, Module II functions as XOR gate and Module III functions as multiplexers.

![Fig 1: basic block diagram.](image1)

These three modules are designed using the hybrid cmos design style, GDI technique, modified GDI, ripple carry adder.

There are three modules in the full adder design they are XNOR-XOR module, sum and carry module. The XNOR/XOR operations on input A and B is performed by the XOR/XNOR module.

![Fig2: Hybrid cmos full adder.](image2)
In the existing system XOR\XNOR module consists of six transistors. Power consumption in full adder is mainly due to the XNOR module. Therefore inverter is used in order to reduce the power consumption of XNOR module. In the carry generator module pass transistors logic gates are present. The delay of the carry signal can be reduced by propagation of the signal through single transmission gate. The transistor count is reduced by using the gate diffusion technique. so that area occupied by the full adder is reduced.

![Output waveform for 1 bit hybrid full adder (14T).](image)

In the 14T hybrid full adder the power consumption is 11.235\mu w and time delay is 8.010ns. Here to get the clear graph without any noise we used time division of 50ns. Gate diffusion technique:

![GDI Basic cell](image)

The basic differences between cmos inverter and GDI cell are

1. There are three inputs G terminal, P terminal, N terminal G-terminal which is common input for both pmos and nmos. P terminal is the input for source or drain of pmos. N terminal is the input for the source and drain of nmos.

2. The nmos and pmos are connected to N or P terminals respectively.

3. The transistor count is reduced by using the gate diffusion technique. In designing of full adder Vdd is connected to P terminal and Ground is connected to N terminal.
In this full adder circuit GDI technique has been used for producing intermediate function of XOR. The energy efficiency is increased when compared with several cmos circuits. The issue of compatibility for twin-well cmos process is currently being explored.

GDI consists of three modules

Fig 5: Design of full adder of 10 transistors using GDI technique.

Module 2 is the operation between A, B, Cin using XOR gate. So that the operation is A XOR B XOR Cin.

In this module selection line is A XOR B. Carry is generated from the inputs A and Ci

Fig 6: XOR\XNOR module.

Fig 7: Output wave form for 1 bit hybrid full adder (10T)
In the hybrid full adder with 10 T the power consumption is 5.765µw and time delay is 8.010ns.

4. Proposed system:

Modified Gate diffusion input:

Fig 8: Modified gate diffusion technique.

In modified GDI, two terminals are present they are Sp, Sn. PMOS node, NMOS node are connected to the Sp, Sn respectively, CMOS are made compatible.

Fig 9: full adder with 8 transistors in 1 bit by using modified gate diffusion technique.

In this full adder we use the modified GDI technique, we reduce the transistor count to 8. Here three modules are present they are XNOR, sum, carry module. Sum module will generate the sum output.

Now design of full adder with 8 bit is done using ripple carry adder technique.

Fig 10: Output wave form for 1bit Hybrid full adder (8T).
In the 14T hybrid full adder the power consumption is 0.005μw and time delay is 8.000ns Table 1: comparison of the 1 bit hybrid full adders Comparison of existing and proposed system.

<table>
<thead>
<tr>
<th>Number of transistors</th>
<th>Technique</th>
<th>Power</th>
<th>Time</th>
</tr>
</thead>
<tbody>
<tr>
<td>14T</td>
<td>CMOS, PTL</td>
<td>0.109mW</td>
<td>8.10 ns</td>
</tr>
<tr>
<td>10T</td>
<td>Gate diffusion</td>
<td>0.107mW</td>
<td>8.10 ns</td>
</tr>
<tr>
<td>8T</td>
<td>Mod-GDI</td>
<td>0.05 mW</td>
<td>8.00nS</td>
</tr>
</tbody>
</table>

5. Design of 8 Bit Hybrid Full adders using Ripple carry adder:

Ripple carry adder:

The N bit parallel data is added by the series of full adders by passing the carry from one full adder to another full adder. So that the carry is rippled from one full adder to other adjacent full adder. Propagation delay in ripple carry adder is considerable since the time delay between the inputs
And output is more for output should be ‘1’ and vice versa the time taken for the NOT gate’s output to become zero after application of logic ‘1’ to the NOT gate’s input is called the propagation delay.

A standard 8-bit ripple-carry adder built as a cascade from eight 1-bit full-adders. Click the input switches or use the following bind keys: (‘c’) for carry-in, (‘a’, ’k’) for A0...A7 and (‘1’, ’2’, ’8’) for B0...B7.

To demonstrate the typical behavior of the ripplecarry adder, very large gate-delays are used for the gates inside the 1-bit adders - resulting in an addition time of about 0.6 seconds per adder.

In the ripple carry adder each stage of hybrid full adder has to wait until the previous stage carry output has to be propagated. The operands like A = 0b0000000, B=0b11111111 or A=0b01010101 and B=0b10101010 (select these, and
then switch carryin to both 0 and 1, and watch the circuit to settle). the total time delay for the ripple carry adder is very high. In case of the 16 or greater bit fast adders are required.

8 bit hybrid full adders (14 T, 10 T, 8 T):

![Fig 12: 8 bit 14 T hybrid full adder.](image)

In the above figure buffer input is given for every 1 bit hybrid full adder to reduce the noise in the full adder. A, B, Cin are the inputs in the 8 bit hybrid full adder. Sum, carry are the outputs in the full adder.

![Fig 13: 8 bit 10 T hybrid full adder.](image)

In the above figure similar buffers are provided for every block in the full adder to reduce the noise.

![Fig 14:8 bit 8 transistors hybrid full adder.](image)

In the 8 bit hybrid ripple carry adder the A, B, Cin inputs are provided for every block in the ripple carry adder. The 1 bit 8T hybrid full adder is converted in to the block. So totally there 8 blocks in 8 bit full adders. The power consumption in 8 bit 8 T full adder greater when compared to 8 bit 10 t full adder.

![Fig 15: Output of 8bit hybrid full adder (14T)](image)
In the 14T 8bit hybrid full adder the power consumption is 27.16mw. The buffer is placed in the circuit to reduce the noise in the 8 bit hybrid ripple carry adder with 14 transistors. The time delay is not displayed since for architectural diagram time delay will not be displayed.

**Fig 16: Output of 8bit hybrid full adder (10T).**

In the 14T 8bit hybrid full adder the power consumption is 9.406mw. The buffer is placed in the Circuit to reduce the noise in the 8 bit hybrid ripple carry adder with 14 transistors. The time delay is not displayed since for architectural diagram time delay will not be displayed.

**Fig 17: Output of 8bit hybrid full adder (8T).**

In the 14T 8bit hybrid full adder the power consumption is 17.581mw. The buffer is placed in the circuit to reduce the noise in the 8 bit hybrid ripple carry adder with 14 transistors. The time delay is not displayed since for architectural diagram time delay will not be displayed. The performance analysis of each hybrid full adder are studied and tabulated. The power consumption of the 14T, 10T, 8T is reduced in order from highest to lowest.

**Table 2: comparison of the existing and proposed full adders.**

<table>
<thead>
<tr>
<th>Number of Transistors</th>
<th>1-BIT</th>
<th>8-BIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>14 T</td>
<td>10 T</td>
</tr>
<tr>
<td>Technique used</td>
<td>Cmos, pass transistor logic</td>
<td>Gate diffusion technique</td>
</tr>
<tr>
<td>Power</td>
<td>11.235μw</td>
<td>5.765μw</td>
</tr>
<tr>
<td>Time delay</td>
<td>8.010ns</td>
<td>8.010ns</td>
</tr>
</tbody>
</table>
Table 3: comparison of 8bit and 1 bit power consumption.

<table>
<thead>
<tr>
<th></th>
<th>1bit power</th>
<th>8 bit power</th>
</tr>
</thead>
<tbody>
<tr>
<td>14 T</td>
<td>11.235µW</td>
<td>27.16 mW</td>
</tr>
<tr>
<td>10 T</td>
<td>5.765 µW</td>
<td>9.406 mW</td>
</tr>
<tr>
<td>8 T</td>
<td>0.005 µW</td>
<td>17.581 mW</td>
</tr>
</tbody>
</table>

5. Conclusion:

The Full adders are designed, such that performance of full adder are increased. The performance measures are validated using the Microwind Simulations are made on the full adders by using CMOS 50 nm technology. The flexibility for designer is provided by using CMOS logic style, GDI technique, and modified gate diffusion technique. The hybrid CMOS full adders operates at different load conditions and at different voltages.

6. References:


3. S. Goel, A. Kumar, and M. A. Bayoumi, “Design of robust, energy efficient full adders for deep sub micrometer design using hybrid-CMOS logic style,”


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